

Nested Dissection Based Parallel Transient Power Grid Analysis on Public Cloud Virtual Machines

Jiawen Cheng, Zhiqiang Liu, Lingjie Li, Wenjian Yu*
 Dept. Computer Science & Tech., BNRist, Tsinghua Univ., Beijing, China.
 Email: cjw21@mails.tsinghua.edu.cn, yu-wj@tsinghua.edu.cn

Abstract—Accurate and efficient transient analysis of power grids (PGs) poses a large challenge of computation for nowadays integrated circuit design. In this work, we propose to leverage the public cloud computing to do PG transient analysis while preserving security. A multi-level distributed parallel LU factorization and forward/backward substitution approach based on nested dissection is then proposed to guarantee accuracy and robustness. Experimental results show that the proposed algorithm can achieve an average 2.06X speedup over NICS LU and 2.85X over conventional domain decomposition method based parallel approach. And, it exhibits good scalability with up to 6.0X parallel speedup on large-scale PGs with 4 cloud computer nodes.

I. INTRODUCTION

Power grid (PG) analysis is increasingly important for designing and verifying the on-chip power delivery system for nowadays low-power integrated circuits (ICs). It includes two kinds of analysis: direct current (DC) analysis and transient analysis. The former regards the PG as a resistive network and ignores capacitors and inductors, while the latter takes them all into account. The major purpose of PG analysis is to compute the voltage drop (i.e. IR drop) at PG nodes under various current load assumptions which reflect different working modes of the circuit. Compared to DC analysis, the transient analysis is more useful to validating the PG design. Due to the increased number of circuit components, the decreased margin for IR drop and the demand of accurate analysis, the transient analysis usually consumes a large portion of time and poses a large challenge of computation for nowadays IC design.

For the transient analysis, a system of first-order ordinary differential equations (ODEs) derived from modified nodal analysis (MNA) need to be solved. With the implicit time integration method, e.g., backward Euler or trapezoidal rule, the problem is converted to the solution of linear equation systems at successive time points. Therefore, the direct solver or iterative solver for sparse linear equation system are employed for efficient PG analysis. The direct solver based method is suitable for transient analysis when the time step is fixed, which only performs the expensive LU or Cholesky factorization of the matrix once at the beginning. The direct sparse solvers which have been used for circuit simulation include SuperLU series [1], CHOLMOD [2], KLU [3], NICS LU [4] and CKTSO [5], etc.

The iterative solver based method is better suited for the cases with variable time steps because its efficiency is hardly affected by the change of coefficient matrices for different time points. It also consumes less memory so that it better scales to larger problems than the direct solver. Popular iterative solver employs the Krylov subspace iterative methods [6] with

various preconditioning techniques like algebraic multigrid method [7], [8], incomplete LU factorization [9] and graph spectral sparsification [10], [11]. Recently, iterative solvers incorporating graph spectral sparsification techniques have demonstrated highly scalable performance for PG analysis. However, their efficiency relies on the quality of preconditioner, which cannot be robust enough on various problems. For achieving high accuracy during a long-time transient analysis, a tight convergence criterion of iterative solver is also required, which degrades the advantage of iterative method over the direct solver based method. Therefore, an efficient and robust method for transient analysis of large PGs is still desired.

Distributed parallel computing and cloud computing are the technology which can break the computation challenges faced by the time-consuming tasks in electronic design automation (EDA). Domain decomposition method (DDM) is a specialized method developed to explore the parallelism in circuit simulation and PG analysis [12], [13], [11]. Existing work mostly consider the DDM based iterative solver for achieving high parallelism for PG analysis. In [13], the parallel DDM is developed for the DC analysis of very large PGs on distributed computing platform. However, it is on a customized cluster with high-speed Infiniband networks.

Nowadays, public cloud computing platforms have become economic and available computing infrastructure facilitating various computation tasks. However, deploying EDA tools to them is not widely accepted due to the concern of security and actual benefit. In this work, we consider leveraging the public cloud computing to expedite the time-consuming transient PG analysis while preserving security and robustness. An efficient distributed parallel algorithm based on nested dissection, a variant of DDM based direct solver, is proposed to accelerate the transient analysis of large-scale PGs, at the small cost of cloud virtual machine rent. The major contributions of this work are as follows.

1) An idea of expediting transient PG analysis with public cloud computing is proposed. With the circuit netlist parsed locally and the matrices and the source waveforms uploaded to cloud computing platform, it guarantees the security.

2) A multi-level distributed parallel LU factorization algorithm and forward/backward substitution algorithm based on nested dissection is proposed. The relatively small size of the interfaces at each level allows for better parallelism. And, its nature of the direct solver guarantees accuracy and robustness.

3) Only a few vectors are transferred between the processes at each time point of forward/backward substitution, which yields a low communication volume. Therefore, the proposed

algorithm can be deployed on a cloud virtual machine cluster without high-speed networks such as InfiniBand.

4) An efficient scheme is designed for updating the right-hand side (RHS) of the linear system in parallel at each time point. It takes advantage of the fact that processes on the same computer node can share memory. This scheme further reduces computation and communication overhead.

Experiments on transient analysis of 9 practical PGs are conducted on a public cloud computing platform with Ethernet. The results show that the proposed algorithm achieves an average 2.06X speedup compared to NICSLU on a single computer node and an average 2.84X speedup compared to DDM on multiple computer nodes. And, the proposed algorithm exhibits good scalability, with up to 6.0X speedup over the serial simulation on the large-scale PGs.

II. PRELIMINARIES

A. Transient Analysis of Power Grid

In the transient analysis, the PG is modeled as a resistor-inductor-capacitor (RLC) network. Fig. 1 presents a schematic illustration of the detailed RLC model of IBM PG [14].

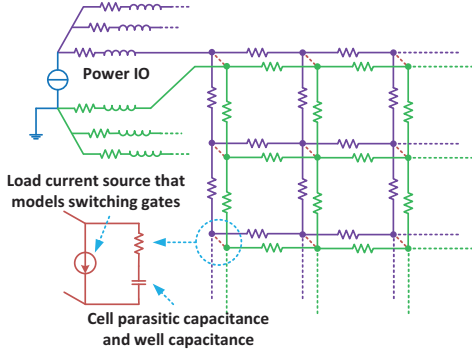


Fig. 1. The RLC model of IBM PG [15].

The ODE system derived from MNA can be formulated as

$$\mathbf{C}\dot{\mathbf{x}}(t) + \mathbf{G}\mathbf{x}(t) = \mathbf{B}\mathbf{u}(t), \quad (1)$$

where $\mathbf{C} \in \mathbb{R}^{n \times n}$, $\mathbf{G} \in \mathbb{R}^{n \times n}$, $\mathbf{B} \in \mathbb{R}^{n \times p}$ denote the capacitance and inductance matrix, conductance matrix, and input selector matrix, respectively. $\mathbf{u}(t) \in \mathbb{R}^p$ represents the vector of p input sources and $\mathbf{x}(t) \in \mathbb{R}^n$ represents the solution vector of node voltages and branch currents.

By applying the trapezoidal rule, one can convert (1) into the task of solving the following linear equation system at each time point.

$$\left(\frac{\mathbf{C}}{h} + \frac{\mathbf{G}}{2}\right)\mathbf{x}(t+h) = \left(\frac{\mathbf{C}}{h} - \frac{\mathbf{G}}{2}\right)\mathbf{x}(t) + \mathbf{B}\frac{\mathbf{u}(t+h) + \mathbf{u}(t)}{2}, \quad (2)$$

where h is the time step in transient analysis. We can further use \mathbf{A} to denote $\frac{\mathbf{C}}{h} + \frac{\mathbf{G}}{2}$ and \mathbf{b} to denote the RHS in (2). So, (2) is rewritten as $\mathbf{A}\mathbf{x} = \mathbf{b}$. When h is fixed, matrix \mathbf{A} is a constant at different time points, so that applying the direct solver is preferred as only one expensive matrix factorization is required.

B. Domain Decomposition Method

Domain decomposition method (DDM) refers to a series of divide-and-conquer techniques based on graph partitioning for solving linear equations [12]. In this work, we focus on the DDM aided direct solver for symmetric linear equations $\mathbf{A}\mathbf{x} = \mathbf{b}$, instead of the DDM based iterative solver. The symmetric

matrix \mathbf{A} naturally corresponds to an undirected graph. As shown in Fig. 2, the DDM can be realized with two kinds of separators: edge separator and vertex separator. The edge separator is an edge subset satisfying that the removal of it makes the graph divided into m unconnected components of similar size called subdomains. The vertex separator is defined similarly. The separator nodes are also known as the interface.

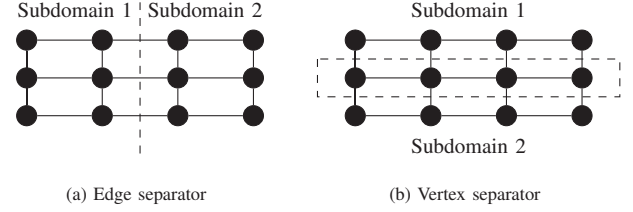


Fig. 2. An example of partitioning a graph into two subdomains with (a) an edge separator or (b) a vertex separator.

The DDM with edge or vertex separator is widely recognized as the graph partitioning problem. Suppose the graph is partitioned into m subdomains. For any value of m , it can be efficiently solved with algorithms like METIS [16]. When $m = 2$, the DDM with vertex separator forms a dissection of vertices. When it is recursively executed for each subdomain, the nested dissection enables an effective reordering approach for sparse direct solver [17].

With DDM, the $\mathbf{A}\mathbf{x} = \mathbf{b}$ problem can be rewritten as the equation with blocked sparse coefficient matrix:

$$\begin{pmatrix} D_1 & & & F_1 \\ & D_2 & & F_2 \\ & & \ddots & \vdots \\ & & & D_m & F_m \\ E_1 & E_2 & \cdots & E_m & S \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ \vdots \\ x_m \\ \mathbf{y} \end{pmatrix} = \begin{pmatrix} f_1 \\ f_2 \\ \vdots \\ f_m \\ \mathbf{g} \end{pmatrix}, \quad (3)$$

where the internal nodes in each subdomain correspond to the diagonal blocks D_1, D_2, \dots, D_m , and S corresponds to the separator nodes. Connection matrices $E_i = F_i^T, i = 1, \dots, m$ reflect the connections between the internal nodes and the separator nodes.

To simplify notation, we rewrite (3) as

$$\begin{pmatrix} \mathbf{D} & \mathbf{F} \\ \mathbf{E} & \mathbf{S} \end{pmatrix} \begin{pmatrix} \mathbf{x} \\ \mathbf{y} \end{pmatrix} = \begin{pmatrix} \mathbf{f} \\ \mathbf{g} \end{pmatrix}, \quad (4)$$

where \mathbf{D} is a block diagonal matrix. By eliminating all internal nodes, (4) becomes

$$(\mathbf{S} - \mathbf{E}\mathbf{D}^{-1}\mathbf{F})\mathbf{y} = \mathbf{g} - \mathbf{E}\mathbf{D}^{-1}\mathbf{f}. \quad (5)$$

The dense matrix $\mathbf{S} - \mathbf{E}\mathbf{D}^{-1}\mathbf{F}$ is called the Schur complement matrix. Finally, the internal unknowns can be solved with

$$D_i \mathbf{x}_i = \mathbf{f} - \mathbf{F}_i \mathbf{y}. \quad (6)$$

The opportunities for parallelism are solving $\mathbf{D}^{-1}\mathbf{F}$, $\mathbf{D}^{-1}\mathbf{f}$ and (6). As the number of subdomains m increases, the size of the interface also increase and solving (5) becomes a computational bottleneck. The above analysis also works for the DDM with edge separator, where the size of Schur complement is even larger. In [11], the DDM with edge separator is employed to parallelly solve the preconditioner matrix in the iterative solver based method. However, the DDM based parallel direct solver for PG analysis is less explored.

III. METHODOLOGY

In order not to expose the internal structure of circuit, its netlist should be parsed locally. Then, according to (2), the data uploaded to the public cloud computing platform are the matrices C, G, B , the source waveforms $u(t)$ and the initial state of x . The coefficient matrix $\frac{C}{h} + \frac{G}{2}$ is symmetric but not necessarily positive definite. Therefore, an LU factorization based on nested dissection is performed on it, followed by a forward/backward substitution and an RHS updating at each time step.

A. The Idea of Using Nested Dissection

Since DDM forms a large dense Schur complement with many subdomains, we consider recursive partitioning of the matrix inspired by nested dissection. In this way, the size of the interface can be effectively reduced, which can improve the parallel efficiency. Specifically, consider a matrix partitioned into two subdomains and an interface. After reordering, its LU factorization should satisfy

$$\begin{pmatrix} D_1 & F_1 \\ D_2 & F_2 \\ E_1 & E_2 & S \end{pmatrix} = \begin{pmatrix} L_{11} & & \\ & L_{22} & \\ L_{31} & L_{32} & L_{33} \end{pmatrix} \begin{pmatrix} U_{11} & U_{13} \\ & U_{22} & U_{23} \\ & & U_{33} \end{pmatrix}. \quad (7)$$

Suppose the LU factorization of D_1, D_2 is known, then the unknowns in L and U factors can be solved by

$$L_{31} = E_1 U_{11}^{-1}, L_{32} = E_2 U_{22}^{-1}, \quad (8)$$

$$U_{13} = L_{11}^{-1} F_1, U_{23} = L_{22}^{-1} F_2, \quad (9)$$

and a LU factorization of the Schur complement

$$L_{33} U_{33} = S - L_{31} U_{13} - L_{32} U_{23}. \quad (10)$$

The factorization of D_1, D_2 can be done recursively in the same manner, so that the coefficient matrix is reordered into the form of nest dissection. The opportunities for distributed parallelism are the factorization of D_1, D_2 , the solution of (8) and the solution of (9). The factorization of the Schur complement is executed on a single process, but the cost is acceptable because of its relatively small size.

For forward substitution, the equations to be solved is

$$\begin{pmatrix} L_{11} & & \\ & L_{22} & \\ L_{31} & L_{32} & L_{33} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \\ y \end{pmatrix} = \begin{pmatrix} f_1 \\ f_2 \\ g \end{pmatrix}. \quad (11)$$

The solution can be obtained by solving

$$L_{11} x_1 = f_1, L_{22} x_2 = f_2, L_{33} y = g - L_{31} x_1 - L_{32} x_2. \quad (12)$$

Because L_{11}, L_{22} conform the nested dissection form, the solution of x_1, x_2 can be performed recursively in parallel. The solution of x_3 is performed on a single process. For backward substitution, the solution can be obtained similarly.

B. Parallel Reordering and Factorization

To reorder the matrix into the nested dissection form, a multi-level parallel algorithm is adopted. Suppose the maximum nested level is l_m , then the total number of processes is 2^{l_m} . For the top level l_m , only process 0 partitions and reorders the entire matrix. For the next level $l_m - 1$, process 0 and process 2^{l_m-1} partition each of the two subdomains derived from the level l_m in parallel. The matrix reordering proceeds similarly for the remaining levels except level 0. For level l , processes whose numbers divide 2^l can perform matrix partitioning in parallel. For level 0, a permutation vector is computed for reducing fill-ins. Fig. 3 illustrates an example

of task assignment for 3-level matrix reordering, where the number in each node indicates the number of the process executing the task.

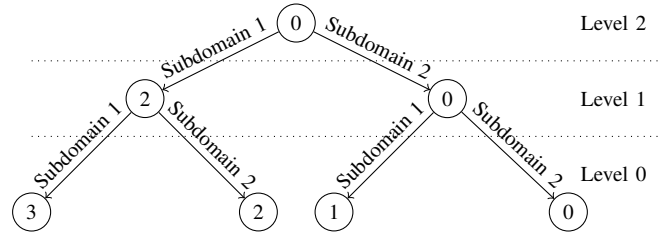


Fig. 3. An example of task assignment for 3-level matrix reordering.

The above matrix reordering algorithm is summarized as Algorithm 1. Given the maximum nested level l_m , the algorithm uses four vectors f, g, h, e of length $l_m + 1$ to record partition information of each level for subsequent factorization and solving, where f, g, h denote the offsets of subdomain 1, subdomain 2 and the interface in the entire matrix, respectively, and e denotes the end of the submatrix. The superscript (r) means the data resides in process r and the subscript l means the data describes information of level l .

Algorithm 1 Parallely reorder A with the nested dissection approach

Input: Matrix A , nested level l_m .

Output: Partition vectors $f^{(r)}, g^{(r)}, h^{(r)}, e^{(r)}$, reordered matrix A .

- 1: $A^{(0)} \leftarrow A$.
- 2: **for** each process r **do**
- 3: Initialize 4 integer vectors $f^{(r)}, g^{(r)}, h^{(r)}, e^{(r)}$, each of length $l_m + 1$ and filled with 0.
- 4: Initialize an empty local permutation vector $p^{(r)}$.
- 5: **for** $l = l_m$ to 1 **do**
- 6: **if** r divides 2^l **then**
- 7: Compute the vertex separator of $A^{(r)}$ to obtain vectors P_1, P_2, S , which stand for the indices of the separated parts and the vertex separator, respectively.
- 8: Prepend S to $p^{(r)}$.
- 9: $g_l^{(r)} \leftarrow f_l^{(r)} + |P_1|, h_l^{(r)} \leftarrow g_l^{(r)} + |P_2|$.
- 10: $e_l^{(r)} \leftarrow f_l^{(r)} + \text{NROW}(A^{(r)})$.
- 11: Send matrix $A^{(r)}(P_1, P_1)$ and integer $f_l^{(r)}$ to process $r + 2^{l-1}$. \triangleright send subdomain 1 to left child
- 12: $A^{(r)} \leftarrow A^{(r)}(P_2, P_2), f_{l-1}^{(r)} \leftarrow g_l^{(r)}$.
- 13: Broadcast $f_l^{(r)}, g_l^{(r)}, h_l^{(r)}, e_l^{(r)}$ to process $r + 1, r + 2, \dots, r + 2^l - 1$.
- 14: **else if** r divides 2^{l-1} **then**
- 15: $A^{(r)}, f_{l-1}^{(r)} \leftarrow$ matrix and integer received from process $r - 2^{l-1}$. \triangleright receive subdomain 1 from parent
- 16: Compute fill-in reducing permutation vector p_f for $A^{(r)}$.
- 17: Prepend p_f to $p^{(r)}$.
- 18: $e_0^{(r)} \leftarrow f_0^{(r)} + \text{NROW}(A^{(r)})$.
- 19: Gather $p^{(r)}$ to all processes and obtain p .
- 20: Reorder A with p .

For the DDM and the proposed algorithm, each process is allocated two threads (i.e., two CPU cores).

The results on a single computer node are listed in Table I. Because the scale of thupg8t and thupg10t is too large, all three implementations fail to complete the simulation due to out of memory. From the results we see that the proposed algorithm achieves an average 2.06X speedup over NICSLU and an average 1.43X speedup over the DDM.

TABLE I
RESULTS OF TRANSIENT POWER GRID ANALYSIS ON A SINGLE COMPUTER NODE (TIME IN UNIT OF SECOND)

Case	N_{th}	NICSLU		DDM				Proposed			
		T_s	T	T_f	T	N_S	T_f	T	\bar{N}_S	Sp1	Sp2
ibmpg3t $N = 1.0E6$ $nnz = 4.5E6$	4	47.8	9.07	24.8	0	8.88	25.9	0	1.84	0.96	
	8	40.7	5.60	18.5	2325	6.08	16.3	561	2.49	1.13	
	16	32.2	5.43	23.1	6288	4.25	13.1	377	2.45	1.76	
	32	34.8	5.47	27.3	10860	3.83	10.6	261	3.30	2.58	
ibmpg4t $N = 1.2E6$ $nnz = 5.8E6$	4	56.2	12.6	34.4	0	12.3	34.5	0	1.63	1.00	
	8	43.1	7.82	24.9	3334	9.13	25.0	723	1.72	0.99	
	16	37.3	6.51	27.2	6410	5.55	16.4	335	2.28	1.66	
	32	41.9	8.43	39.1	13112	4.79	14.6	353	2.86	2.67	
ibmpg5t $N = 1.6E6$ $nnz = 6.4E6$	4	50.1	11.1	32.5	540	11.43	39.2	0	1.28	0.83	
	8	40.1	6.87	23.4	2469	6.87	23.6	330	1.70	0.99	
	16	36.0	5.78	23.7	4670	5.78	16.7	204	2.15	1.41	
	32	43.8	5.25	26.9	9388	5.25	13.9	294	3.15	1.93	
ibmpg6t $N = 2.4E6$ $nnz = 9.7E6$	4	68.9	12.8	40.0	0	12.8	39.2	0	1.76	1.02	
	8	53.2	7.64	27.8	1864	7.64	30.4	266	1.75	0.91	
	16	48.3	5.23	23.7	4178	5.23	22.9	296	2.11	1.04	
	32	61.6	4.51	22.6	7309	4.51	20.6	167	2.99	1.10	
thupg1t $N = 5.3E6$ $nnz = 2.3E7$	4	276	66	176	2953	92.5	193	1401	1.43	0.92	
	8	221	87.1	185	8792	66.0	142	1404	1.55	1.30	
	16	187	69.4	166	15064	44.6	95.4	661	1.96	1.74	
	32	200	51.6	170	25981	36.5	80.5	697	2.49	2.12	
thupg3t $N = 1.2E7$ $nnz = 5.4E7$	4	761	213	487	4646	323	610	2270	1.25	0.80	
	8	587	374	611	14110	316	493	2268	1.19	1.24	
	16	539	218	453	23615	168	300	994	1.80	1.51	
	32	599	188	496	41340	138	252	1034	2.38	1.97	
thupg5t $N = 2.0E7$ $nnz = 8.8E7$	4	1932	533	1013	6777	626	1061	3234	1.82	0.95	
	8	1203	511	915	17513	425	695	2445	1.73	1.32	
	16	1058	482	891	30558	327	539	1576	1.96	1.65	
	32	1211	522	1068	51244	263	445	1210	2.72	2.40	
Average	-	-	-	-	-	-	-	-	-	2.06 1.43	

N_{th} denotes the total number of threads used. T_s, T, T_f denote the time of 1-thread serial simulation, parallel simulation and matrix factorization, respectively. N_S denotes the size of interface in DDM. \bar{N}_S denotes the average size of interfaces at level 1 in the proposed algorithm. Sp1, Sp2 denote the speedup ratios of the proposed algorithm over NICSLU and DDM, respectively.

The results on multiple computer nodes (virtual machines) are listed in Table II. Because NICSLU is based on shared memory architecture, it is removed for this comparison. The experiments with 64 and 128 threads are carried out on 2 and 4 computer nodes, respectively. Each computer node is allocated 16 processes. The DDM and the proposed algorithm both fail to complete the simulation of thupg10t on 2 computer nodes with 64 threads due to out of memory. From the results we see that the proposed algorithm achieves a 2.84X speedup averagely over the DDM, which is larger than the 1.43X speedup on a single computer node and proves its better parallel scalability.

From Table I and II we see that the size of Schur complement is reduced with the nested dissection. The communication volume of forward/backward substitution and RHS updating per time point is consistent with the theoretical analysis in Section III-C, which indicates the low communication overhead of the proposed algorithm. And, the communication volume of matrix reordering and factorization is only a small fraction of the total communication volume.

In all the experiments, the results of the proposed algorithm have no error (in double-precision floating-point arithmetic) with respect to the standard solutions obtained by NICSLU, which proves its accuracy. To further demonstrate the parallel

TABLE II
RESULTS OF TRANSIENT POWER GRID ANALYSIS ON MULTIPLE COMPUTER NODES (TIME IN UNIT OF SECOND, COMMUNICATION VOLUME IN UNIT OF GIGABYTE)

Case	N_{th}	DDM			Proposed					
		T_f	T	N_S	T_f	T	\bar{N}_S	V_f	V_{tr}	Sp
ibmpg3t	64	6.67	36.0	17508	3.96	10.9	162	0.50	0.06	3.29
	128	10.2	56.1	26646	4.16	11.5	126	0.93	0.07	4.88
ibmpg4t	64	8.15	45.5	19966	4.47	13.6	196	0.65	0.07	3.35
	128	13.1	64.8	32215	5.01	14.0	172	1.19	0.09	4.63
ibmpg5t	64	5.57	30.8	14865	5.57	13.9	159	0.76	0.09	2.22
	128	10.5	51.3	24295	5.84	14.4	138	1.11	0.12	3.57
ibmpg6t	64	5.73	30.4	14441	5.73	18.2	163	0.77	0.13	1.67
	128	9.98	48.4	22794	6.15	18.9	111	1.50	0.18	2.56
thupg1t	64	40.2	175	38348	31.8	75.0	324	3.14	0.31	2.33
	128	47.8	212	58838	33.2	78.3	315	5.55	0.38	2.71
thupg3t	64	142	472	60959	116	224	516	7.78	0.68	2.10
	128	197	541	91613	108	208	489	13.5	0.88	2.60
thupg5t	64	291	863	77062	224	391	763	12.9	1.13	2.21
	128	371	987	117742	209	368	594	22.3	1.47	2.68
thupg8t $N = 4.1E7$ $nnz = 1.8E8$	64	859	2714	106472	806	1175	1049	27.4	2.33	2.31
	128	801	2875	142819	750	1089	874	47.1	2.97	2.64
thupg10t $N = 6.3E7$ $nnz = 2.7E8$	64	1239	4375	181934	1058	1695	1034	73.0	4.57	2.58
	Average	-	-	-	-	-	-	-	-	2.84

The notations of $N_{th}, T_f, T, N_S, \bar{N}_S$ and Sp are the same as Table I. V_f denotes the communication volume of matrix reordering and factorization and V_{tr} denotes the average communication volume of forward/backward substitution and RHS updating per time point.

scalability of the proposed algorithm, we plot the speedup ratios of the three implementations with different number of threads over 1-thread serial simulation on thupg3t and thupg5t in Fig. 5. From it we see that the speedup ratios of NICSLU and DDM are basically unchanged with the increase of the number of threads, and that of DDM even decreases with 128 threads. In contrast, the speedup ratio of the proposed algorithm increases with the number of threads and achieves up to about 6.0X with 128 threads. The reason is that the proposed algorithm effectively reduces the size of Schur complement and has a low communication volume.

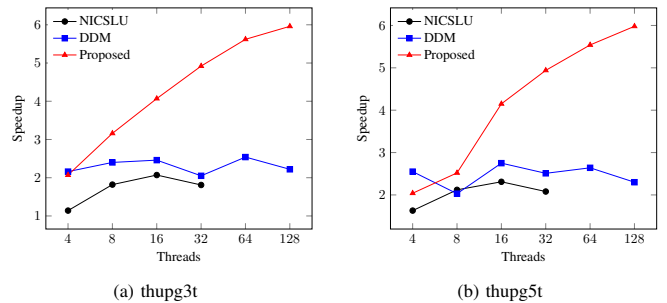


Fig. 5. The speedup ratios of three implementations with different number of threads over 1-thread serial simulation on thupg3t and thupg5t.

Finally, we do a rough cost analysis. In the cloud computing platform, the rental price of the virtual machine we use is 1.62\$/h. For the transient simulation of thupg8t, using 4 computer nodes costs extra $(1089 \times 4 - 1175 \times 2) \times 1.62 / 3600 = 0.90\$$ for virtual machine rent than using 2 computer nodes. On the other hand, this reduces $1175 - 1089 = 86s$ of the simulation time which means saving 86s time of the IC designer. This is beneficial as it corresponds to saving 0.96\$ providing that the human cost of IC designer is about 40\$/h. For larger cases, using the multiple nodes in cloud computing would be the required choice for accurate transient analysis due to its excessive memory cost.

V. CONCLUSIONS

In this work, we propose to leverage the public cloud computing for transient PG analysis while ensuring security. A multi-level distributed parallel LU factorization and forward/backward substitution approach based on nested dissection with low communication overhead is then proposed to guarantee accuracy and robustness. And, an efficient scheme is designed for RHS updating of the linear system to further exploit parallelism. These make the proposed algorithm suitable to be deployed on public cloud computing platforms without InfiniBand. Experiments on transient analysis of 9 practical PGs show that the proposed algorithm achieves an average 2.06X speedup over NICS LU on a single computer node and an average 2.84X speedup over DDM on multiple computer nodes. Moreover, the proposed algorithm exhibits good scalability, with up to 6.0X speedup over the serial simulation on the large-scale power grids.

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