Efficient Capacitance Modeling and Extraction for the Cylindrical Inter-Tier-Vias in 3-D ICs

Wenjian Yu

Department of Computer Science & Technology,
Tsinghua University, Beijing 100084, China

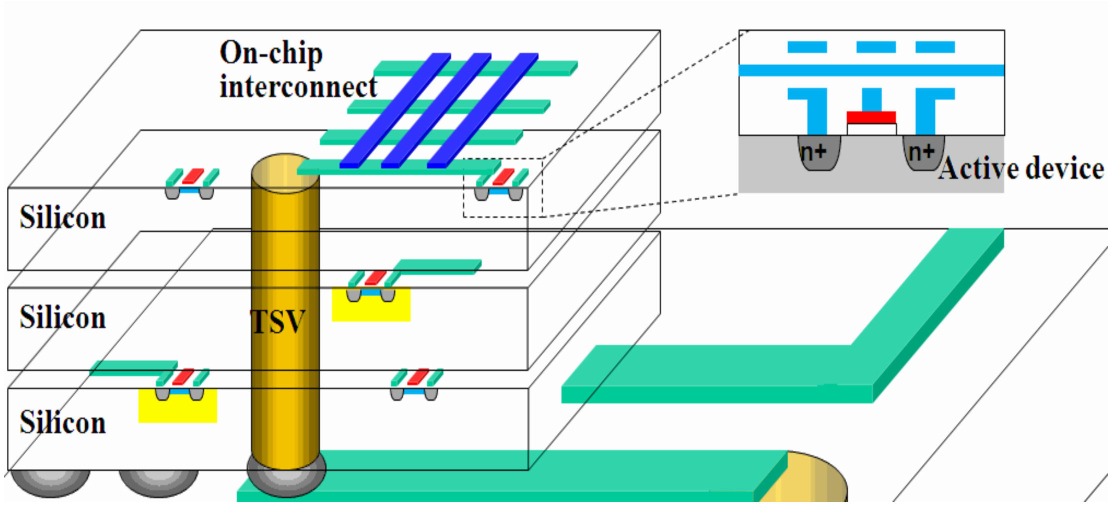
Dec. 16, 2017

Outline

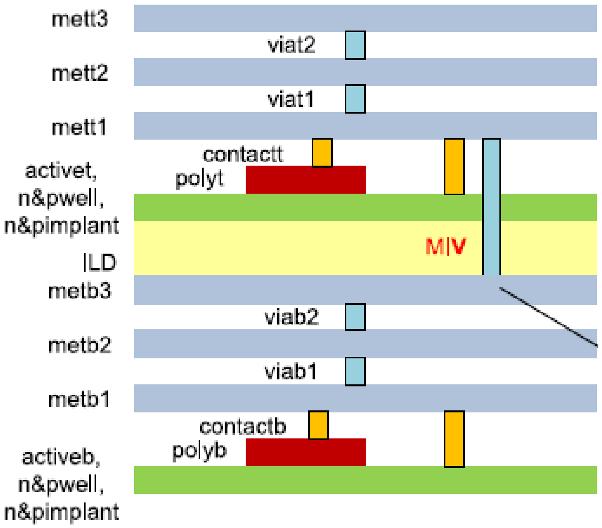
- Background and motivation
- The floating random walk algorithm for capacitance extraction
- FRW based technique for the cylindrical ITVs
- Comprehensive modeling of TSVs in 3-D IC
- Conclusions

Background

- 3-D IC: a promising solution offering a path beyond the Moore's law
- Two types of vertical integrating for 3-D IC
  - Die stacking using through-silicon-via (TSV)
  - Monolithic integration using monolithic inter-tier-via (MIV)



TSV in die-stacking 3-D IC



MIV in monolithic 3-D IC [1]

[1] **S. Panth**, et al., "High-density integration of functional modules using monolithic 3D-IC technology," ***ASP-DAC* 2013**

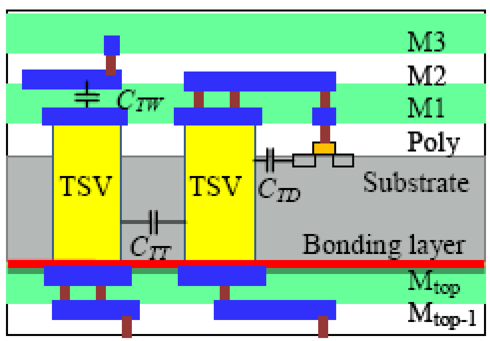
Background

- The problem
  - The inter-tier-vias (viz. TSV and MIV) play a critical role in 3-D ICs to deliver signal and power
  - Their related parasitics need accurate modeling (rising number of analog effects, narrowed performance margins)
- Extraction of ITV capacitances
  - Most works focused on TSV's equivalent model and its *MOS capacitance*, instead of the *electrostatic coupling* among TSVs and horizontal wires
  - [T-CPMT 2011][1] reveals the electrostatic cap. can be comparable to the MOS cap.; The *analytical* technique is based on square-shape TSV, and has >20% error

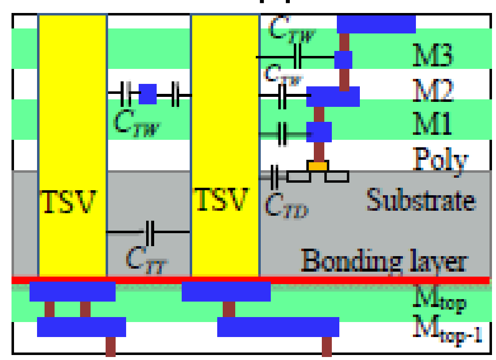
[1] **D. H. Kim**, et al., "Fast and accurate analytical modeling of through-silicon-via capacitive coupling," ***IEEE T-CPMT***, 2011

Background

- Actual ITV is more like a cylinder in geometry
  - TSV-first, TSV-last, TSV-middle, etc.
  - Large size (diameter~5μm), large aspect ratio (~10)
  - In exiting work, calculation of C_{TT} and C_{TD} investigated



TSV-first



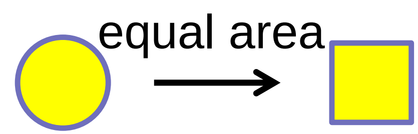
TSV-last

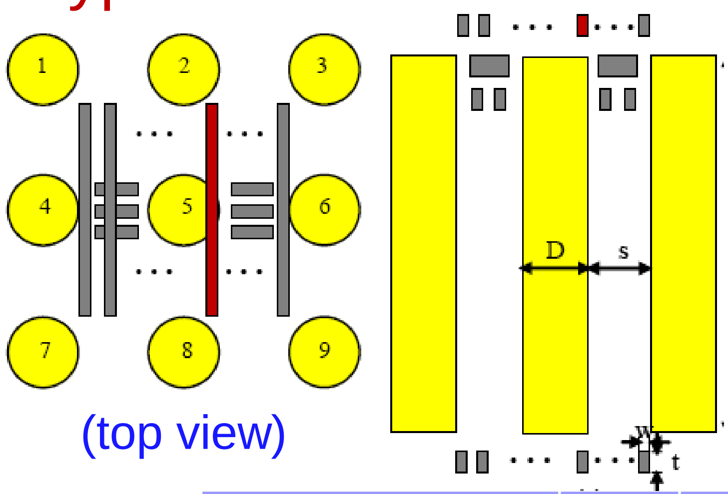
not considering the wires surrounded laterally and vertically

  - Monolithic 3-D IC similar to TSV-first; smaller-size MIV
  - Larger density of MIV; larger aspect ratio than local via

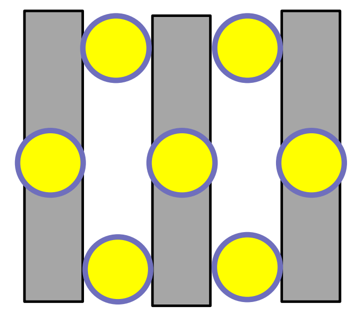
Background

- Cylindrical ITV, or square-shape ITV?
  - The error of square-shape approximation
  - Typical TSV and MIV structures





(top view)



(top view of MIV)

Raphael simulation	C_{total} (aF)		Err. C_{total} (%)	Error of C_{couple} (%)	
	Cylinder	Square		min	max
TSV-first	3740	3962	5.9	-20	21
TSV-last	3866	4065	5.2	-38	71
MIV	14.7	15.8	7.5	-1.6	9.1

Square approximation overestimates C_{total}, while causes large errors on C_{couple}

Background

- High-precision capacitance extraction -- Field Solver
  - Finite difference/finite element method
    - Stable, versatile; slow

      Raphael, Q3D
  - Boundary element method
    - Fast for small/medium size cases

      FastCap, Act3D, QBEM[1]
    - Polyhedron approximation; discretization
  - Floating random walk method

    QuickCap/Rapid3D, RWCap[2]
    - Stable (discretization-free); Scalable (low memory cost),
    - Only efficient for Manhattan structures
- None of the fast solvers directly and efficiently handle the structure with *cylindrical* ITVs

[1] **W. Yu**, et al., "Enhanced QMM-BEM solver for 3-D multiple-dielectric capacitance extraction within finite domain," ***IEEE T-MTT***, 2004

[2] **W. Yu**, et al., "RWCap: A floating random walk solver for 3-D capacitance extraction of VLSI interconnects," ***IEEE T-CAD***, 2013

Background

- Our work
  - The *first* capacitance field solver that can directly handle cylindrical ITVs without any geometric approximation
  - It can be *tens to hundreds times faster* than fast BEM solvers for TSV or large MIV structures, with great memory saving and more stable accuracy
  - It is used in modeling complete electro/semiconductor effects of TSV structures, which results in 47X speedup over a commercial simulator while keeping accuracy

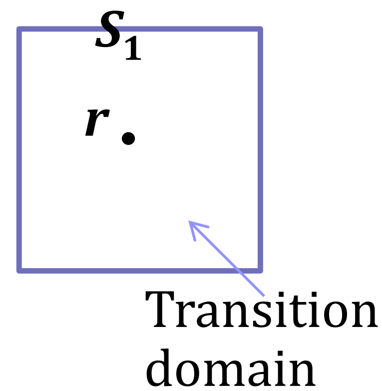
Outline

- Background and motivation
- The floating random walk algorithm for capacitance extraction
- FRW based technique for the cylindrical ITVs
- Comprehensive modeling of TSVs in 3-D IC
- Conclusions

The floating random walk alg.

- Integral formula for the potential calculation

$$\phi(\boldsymbol{r}) = \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)})\phi(\boldsymbol{r}^{(1)})ds^{(1)}$$



P_1 is called surface Green's function, and can be regarded as a probability density function

- Monte Carlo method: $\phi(\boldsymbol{r}) = \frac{1}{M}\sum_{m=1}^{M} \phi_m$

ϕ_m is the potential of a point on S_1, randomly sampled with P_1

- What if ϕ_m is unknown? expand the integral recursively

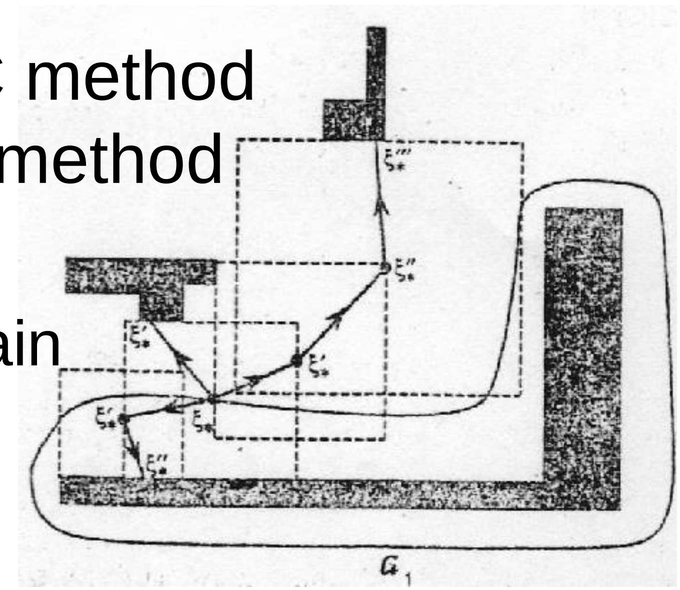
$$\phi(\boldsymbol{r}) = \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)}) \oint_{S_2} P_1(\boldsymbol{r}^{(1)}, \boldsymbol{r}^{(2)}) \cdots$$

$$\oint_{S_k} P_1(\boldsymbol{r}^{(k-1)}, \boldsymbol{r}^{(k)})\phi(\boldsymbol{r}^{(k)})ds^{(k)} \cdots ds^{(2)}ds^{(1)}$$

This spatial sampling procedure is called **floating random walk**

The floating random walk alg.

- The Markov random process + MC method prove the correctness of the FRW method
- A 2-D example with 3 walks
  - Use maximal cubic transition domain
- How to calculate capacitances?



(picture from [1])

Definition: $$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{12} & C_{22} & C_{23} \\ C_{13} & C_{23} & C_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \end{bmatrix}$$

⇒ $Q_1 = C_{11}V_1 + C_{12}V_2 + C_{13}V_3$

Integral for calculating charge (Gauss theorem)

$$Q_1 = \oint_{G_1} F(\mathbf{r}) \cdot \hat{n} \cdot \nabla \phi(\mathbf{r}) d\mathbf{r} = \oint_{G_1} F(\mathbf{r}) \cdot \hat{n} \cdot \nabla \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r}$$

$$= \oint_{G_1} F(\mathbf{r}) g \oint_{S_1} P_1(\mathbf{r}, \mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) \omega(\mathbf{r}, \mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r}$$

weight value, estimate of C_{11}, C_{12}, C_{13} coefficients

[1] **Y. Le Coz**, et al., "A stochastic algorithm for high speed capacitance extraction in integrated circuits," ***Solid-State Electronics***, 1992

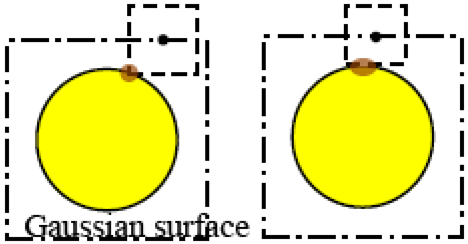
Outline

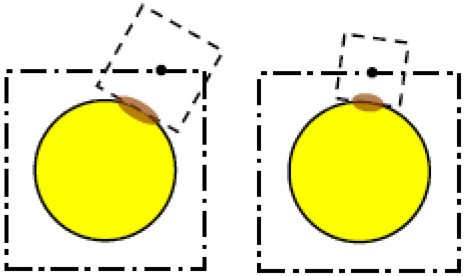
- Background and motivation
- The floating random walk algorithm for capacitance extraction
- FRW based technique for the cylindrical ITVs
- Comprehensive modeling of TSVs in 3-D IC
- Conclusions

Techniques for cylindrical ITVs

- Runtime of FRW: $T_{total} = N_{walk} \cdot N_{hop} \cdot T_{hop}$
- The ideas
  - Manhattan transition cube → rotated transition cube

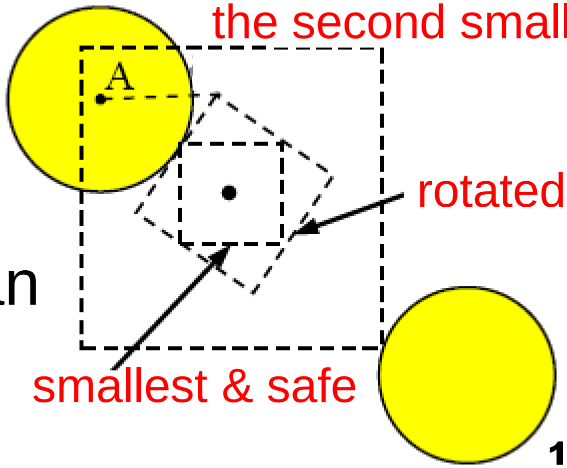
Top view



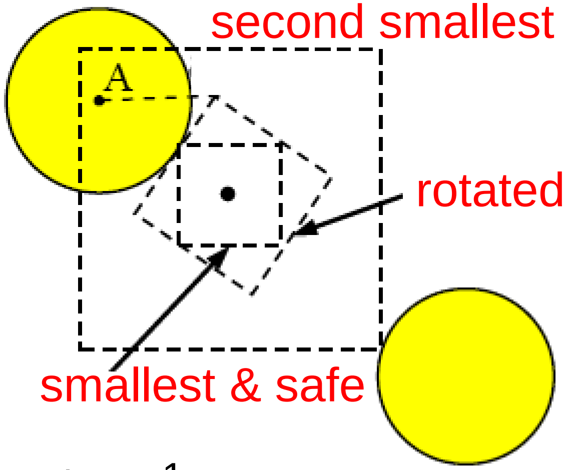


Simple extension of original FRW

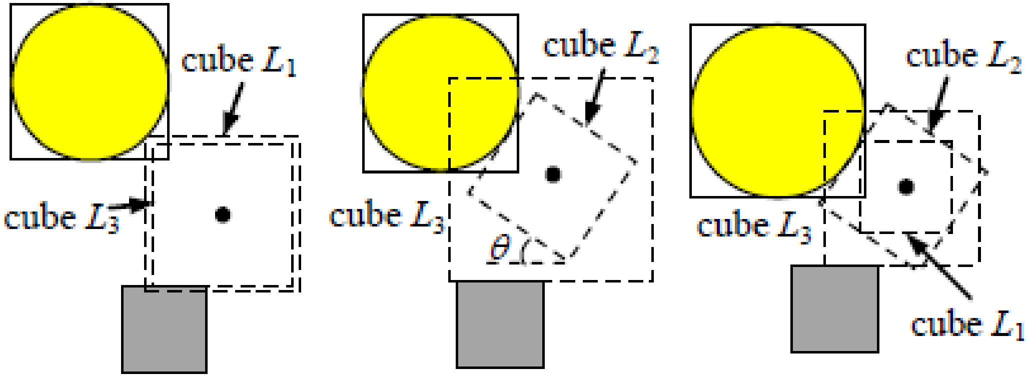
  - Larger probability to terminate; potentially smaller N_{hop}
  - If the rotated cube touching ITV is within the second smallest Manhattan cube, choose the rotated



Techniques for cylindrical ITVs



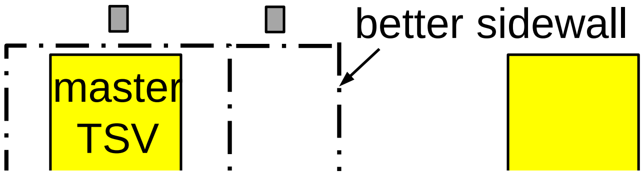
- The ideas
  - Traversing all cylinders increases T_{hop} for cases with many ITVs !
  - Special space management
    - Add ITV's bounding boxes to the conventional space management structure[1]
    - The nearest block is ITV's: may use the rotated cube
    - With the second nearest block, choose valid transition cube



By setting ITV's neighbor region, we can either get the second nearest block efficiently or have a large enough transition cube

[1] **C. Zhang**, et al., "Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks," ***IEEE T-CAD***, 2013

Techniques for cylindrical ITVs



- The ideas
  - Optimized Gaussian surface and importance sampling for TSV structure
    - Setting Gaussian surface the equidistance positions is preferred, but induces large variance to the weight value

$$I_k = \int_{\Gamma_{j,k}} gF(\mathbf{r}) \int_{S_a} -\frac{K_a}{gL(\mathbf{r})} q_a(\mathbf{r},\mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r}$$

Weight value: $\omega_a(\mathbf{r},\mathbf{r}^{(1)}) = -\frac{K_a}{gL(\mathbf{r})}$

$D(\mathbf{r})$ is the distance from $\mathbf{r}$ to TSV

$$I_k = A' \int_{\Gamma_{j,k}} \frac{F(\mathbf{r})}{A'D(\mathbf{r})} \cdot gD(\mathbf{r}) \int_{S_a} -\frac{K_a}{gL(\mathbf{r})} q_a(\mathbf{r},\mathbf{r}^{(1)}) \phi(\mathbf{r}^{(1)}) d\mathbf{r}^{(1)} d\mathbf{r}$$

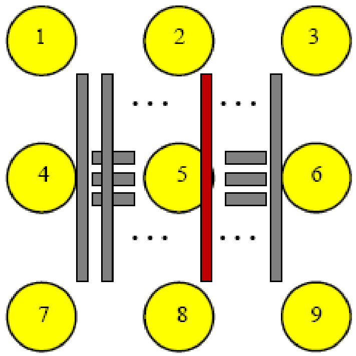
$$\omega_a(\mathbf{r},\mathbf{r}^{(1)}) = -\frac{A'K_a D(\mathbf{r})}{L(\mathbf{r})}$$

    - With compensation of $D(\mathbf{r})$, the variance largely reduced
    - Analytical integral is derived for $A' = \int_{G_j} \frac{F(\mathbf{r})}{D(\mathbf{r})} d\mathbf{r}$
    - Sampling on Gaussian surface with new probability density function finally accelerates the convergence rate for 10X

Techniques for cylindrical ITVs

- Experimental results
  - Accuracy

		Raphael (aF)			newFRW(aF)	
		cylinder	square	Err	cylinder	Err
0.5% criterion	TSV-first(C_t)	3740	3962	5.9%	3793	1.4%
	TSV-last(C_t)	3866	4065	5.1%	3885	0.5%
	MIV(C_t)	14.7	15.8	7.5%	14.8	0.7%
1% criterion	TSV-first(C_c)	49.9	60.2	21%	50.0	0.2%
	TSV-last(C_c)	48.2	58.6	22%	47.9	-0.6%
	MIV(C_c)	2.06	2.24	8.7%	2.12	2.9%



  - Runtime

	oldFRW	newFRW	
	square	cylinder	Inc.
TSV-first(C_t)	2.06	1.66	-19%
TSV-last(C_t)	2.01	2.79	39%
MIV(C_t)	0.61	1.88	3.1X
TSV-first(C_c)	3.5	4.22	21%
TSV-last(C_c)	4.2	5.11	22%
MIV(C_c)	2.6	6.83	2.6X

- The proposed technique scarifies affordable runtime to achieve higher accuracy

Techniques for cylindrical ITVs

- Experimental results
  - Comparison with fast BEMs

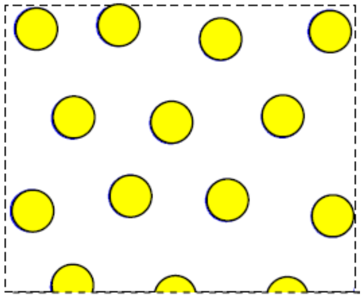
Favorable speedup
Huge memory save

	FastCap*			QBEM*			newFRW			
	Err	time(s)	Mem.	Err	time(s)	Mem.	time(s)	Mem.	Sp1	Sp2
TSV-first(C_t)	-0.8%	67.3	1.8GB	-3.7%	402	7.6GB	1.66	~1MB	40	242
TSV-last(C_t)	-3.4%	79	1.9GB	-4.1%	404	7.7GB	2.79	~1MB	28	145
TSV-first(C_c)	30%	67.3	1.8GB	-3.8%	298	5.9GB	4.22	~1MB	18	71
TSV-last(C_c)	34%	79	1.9GB	-4.4%	299	6.0GB	5.11	~1MB	16	59

*approximate cylinder with 16-side prism

  - Scalability to large-scale cases

	FRW(non-rotate)			newFRW			
	N_{walk}	N_{hop}	time(s)	N_{walk}	N_{hop}	time(s)	Sp.
TSV-first	2.3M	37.6	42.0	2.3M	11.8	1.66	**25**
TSV-last	2.2M	37.4	36.1	2.2M	11.8	2.79	**13**
MIV	224K	23.6	2.08	241K	16.7	1.88	**1.1**
100TSV	6.0M	36.0	231	6.0M	11.5	2.64	**88**
400TSV	6.0M	36.0	710	5.9M	11.5	3.09	**230**
576MIV	149K	13.0	11.4	152K	11.2	1.5	**7.7**



random TSV layout

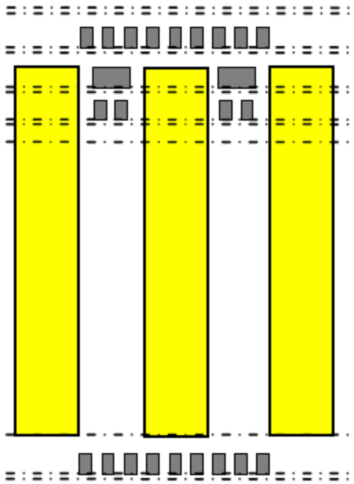
Techniques for cylindrical ITVs

- Experimental results
  - For large-scale cases, Raphael and FastCap don't work due to runtime and memory usage limitations
  - For case 576MIV, FRW is 192X faster than QBEM
  - Multi-dielectric cases
    - Speedup to QBEM is up to 143X

	QBEM			newFRW				
	Cap.	Mem.	Time(s)	Cap.	Error	Mem.	Time(s)	Sp.
TSV-first	32.56	11GB	534	33.9	1.5%	22MB	3.73	**143**
TSV-last	30.96	5.2GB	188	33.2	0.9%	22MB	8.04	**23**
MIV	0.146	581MB	18.4	0.148	1.4%	22MB	2.33	**7.8**
TSV-first2	31.88	8.8GB	400	33.5	1.9%	22MB	7.62	**52**
144MIV	0.276	856MB	35.9	0.292	--	23MB	6.33	**5.7**
576MIV	0.29	6.7GB	344	0.291	--	25MB	5.69	**60**

    - Verified accuracy with Raphael

Multi-layered dielectrics



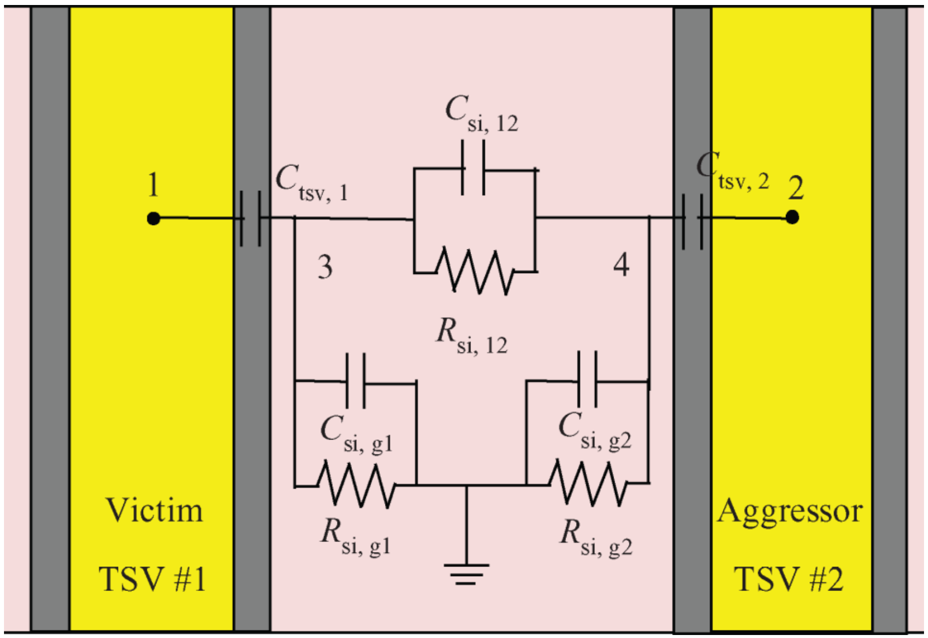
For pre-built GFTs and WVTs

Outline

- Background and motivation
- The floating random walk algorithm for capacitance extraction
- FRW based technique for the cylindrical TSVs
- Comprehensive modeling of TSVs in 3-D IC
- Conclusions

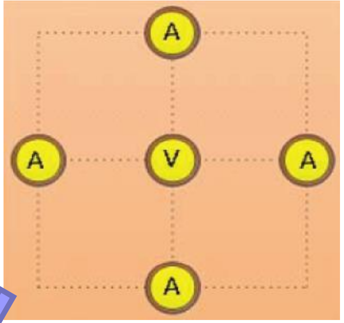
Comprehensive modeling of TSVs

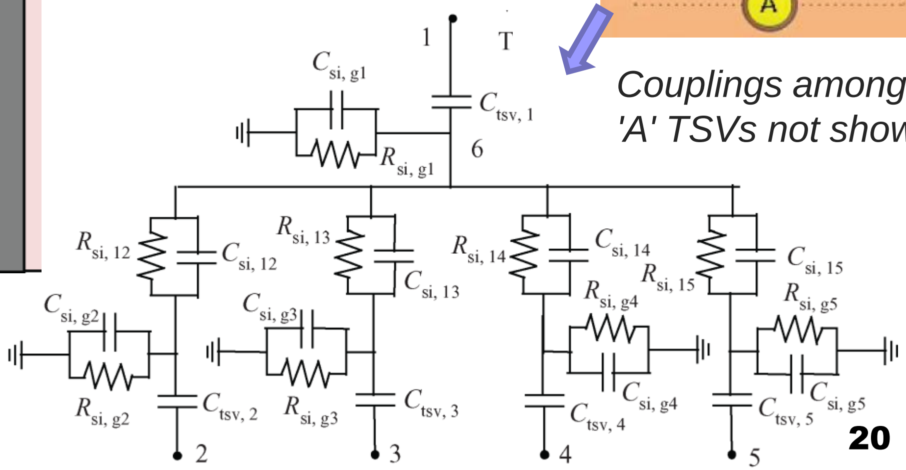
- RC circuit model for analyzing the signal integrity on TSVs (e.g. on a "victim" TSV)
  - Considers both electrostatic and semiconductor effects



A two-TSV structure

- C_{si}: electrostatic cap.
- C_{tsv}: MOS cap.
- $R_{si} = \dfrac{\varepsilon_{si}}{\sigma_{si} C_{si}}$





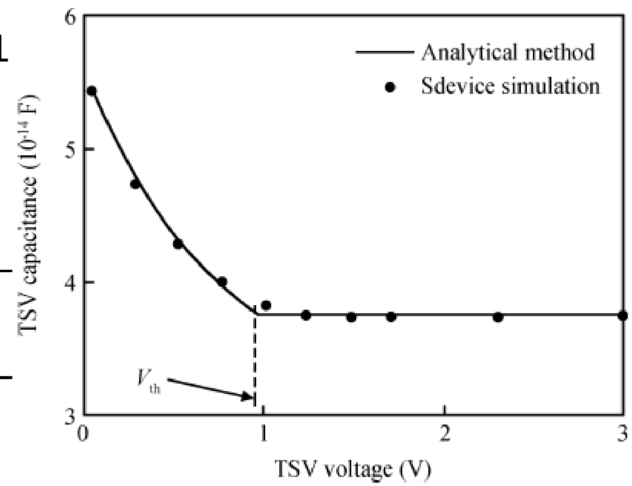
Couplings among 'A' TSVs not shown

Comprehensive modeling of TSVs

- Extraction algorithm flow
  - Input geometry/material information, the voltages of TSVs
  - Extract C_{si}'s with the FRW based capacitance solver
  - Extract C_{TSV}'s with an analytical method[1]
- An algorithm calculating the total lump capacitance of a victim TSV

Input: Equivalent RC circuit of the structure, signal frequency ω;
Ouput: The total lump capacitance of victim TSV C_1.

1. $Y_m = j\omega C_{si,\,g1} + 1/R_{si,\,g1}$;
2. For ($i=2$; $i \le n$; i++) // n is the number of TSVs
   $Y_i = j\omega C_{tsv,i} + j\omega C_{sig,i} + 1/R_{sig,i}$;
   $Y_m = Y_m + (j\omega C_{si,1i} + 1/R_{si,1i})Y_i/(j\omega C_{si,1i} + 1/R_{si,1i} + Y_i)$;
   EndFor;
3. $Y_1 = j\omega C_{tsv,1} Y_m/(j\omega C_{tsv,1} + Y_m)$;
4. $C_1 = \mathrm{real}(Y_1/(j\omega))$;



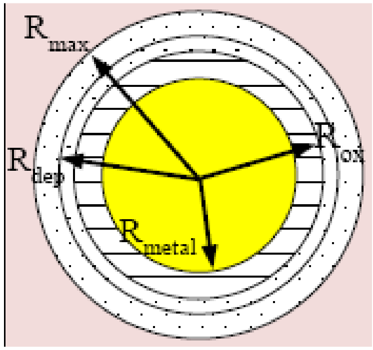
Suitable for arbitrary TSV/ interconnect layout

[1] **G. Katti**, et al., "Electrical modeling and characterization of through silicon via for three-dimensional ICs," ***IEEE Trans Electron Devices***, 2010

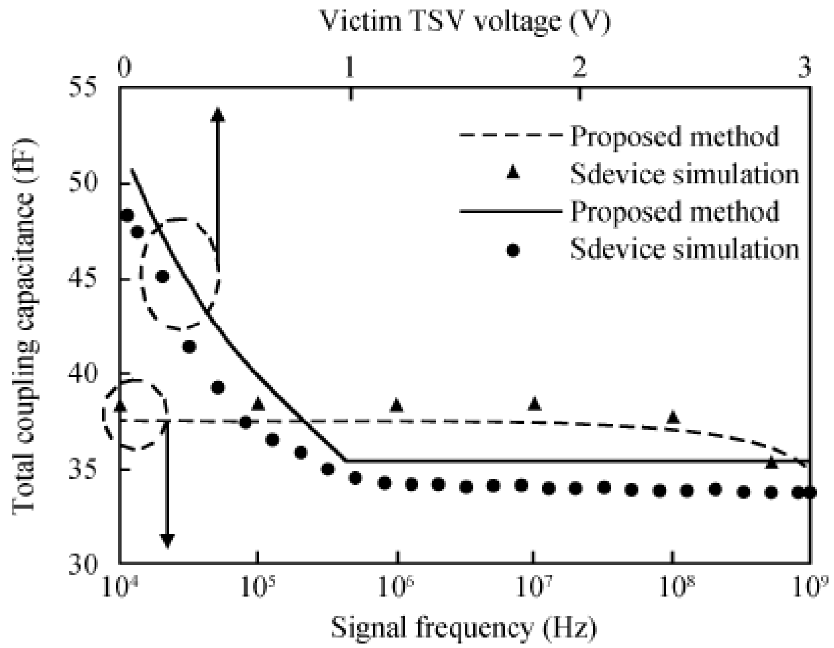
Comprehensive modeling of TSVs

- Experimental results
  - Copper TSVs embedded in a P-Si substrate

R_{metal} (μm)	R_{ox} (μm)	l_{TSV}(μm)	N_a (cm^{-3})
2.5	2.6182	20	2×10^{15}



  - Compared with Sdevice, using FEM for electro/semi simulation
- Results for structures with multiple TSVs



- Capacitance trends vs. f and V_{TSV}
- Error is within 5%

~ 47X speedup in runtime comparison

Case	Sdevice		Proposed method	
	#Grid	Time(s)	Time(s)	Speedup
2-TSV	3476	52.5	159.7	0.33X
5-TSV	8464	147.8	13.8	11X
9-TSV	14562	236.3	5.0	47X

Outline

- Background and motivation
- The floating random walk algorithm for capacitance extraction
- FRW based technique for the cylindrical TSVs
- Comprehensive modeling of TSVs in 3-D IC
- Conclusions

Conclusions

- Extend the FRW algorithm to fast and accurately extract the capacitances of high-density ITVs in 3-D ICs
  - With the *rotated transition cube*, *a special space management* and *an optimized importance sampling* techniques, the proposed method can be over 200X faster than a simple extension of original FRW solver
- The solver is combined with analytical model to simulate electrostatic/semiconductor effects of TSV structures
- Reference

  - Chao Zhang, Wenjian Yu, Qing Wang, and Yiyu Shi, "Fast random walk based capacitance extraction for the 3-D IC structures with cylindrical inter-tier-vias," *IEEE Trans. Computer-Aided Design*, 34(12): 1977-1990, 2015.
  - Qiang Yao, Zuochang Ye, Wenjian Yu, "An efficient method for comprehensive modeling and parasitic extraction of cylindrical through-silicon vias in 3D ICs," *Journal of Semiconductor*, 36(8): 085006-1~7, 2015.

Thank You !

Wenjian Yu / Tsinghua University, China

Codes are shared on

http://numbda.cs.tsinghua.edu.cn

Email: Yu-wj@tsinghua.edu.cn