Efficient Algorithms for Resistance and Capacitance Calculation Problems in the Design of Flat Panel Display

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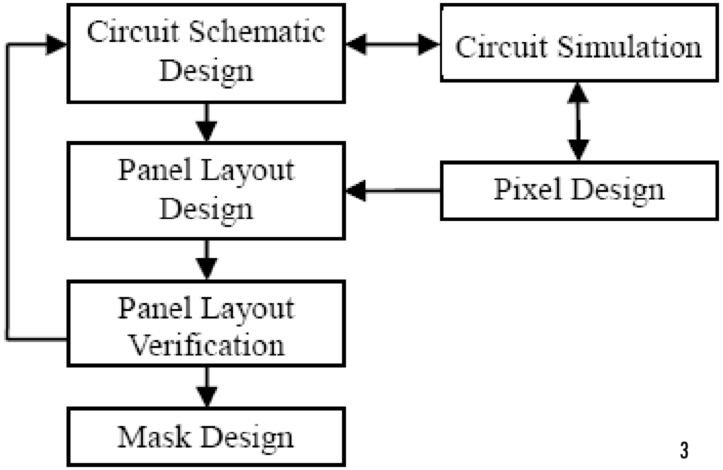
Outline

- Background of FPD Design Automation
- A Hybrid Method for Calculating Wire Resistance
- Floating Random Walk Based Capacitance Solver
- Conclusions

Background

- We are surrounded by FPDs
  - Very-large, high-brightness displays
  - Small-area, high-resolution, low-power
  - Thin-film transistor (TFT) based active matrix technology
  - LCD, OLED with glass/plastic substrate
  - Designing high-performance/low-cost FPDs

- The CAD flow for FPD Design
  - Wire resistance and capacitance need be calculated to validate the signal timing and high display quality



Circuit Schematic Design

Circuit Simulation

Panel Layout Design

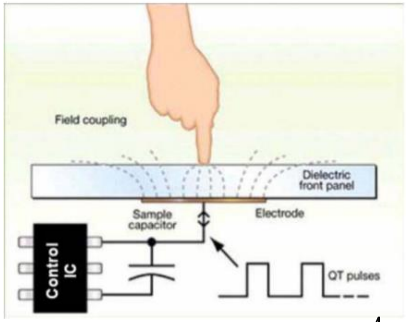
Pixel Design

Panel Layout Verification

Mask Design

Background

- The difference to the parasitic extraction of VLSI circuit
  - The proximity of interconnect wires is less, so that capacitance is smaller and contributes less to signal delay
  - Instead of pursuing small delay, the object in FPD design is keeping almost equal signal delay to display pixels
  - Wire resistance calculation is important
- Touch panel technology
  - Largely enhance the interactivity and user experience
  - TP-FPD includes more complex internal structure
  - Capacitive touch sensor has advantages in durability, reliability and capability
  - Accurate capacitance calculation is needed



Background

- Our contributions
  - A resistance calculation technique for FPD wire design
  - A capacitance calculation technique for TP design
  - They are more efficient than existing techniques, and are applied to actual FPD and TP-FPD designs

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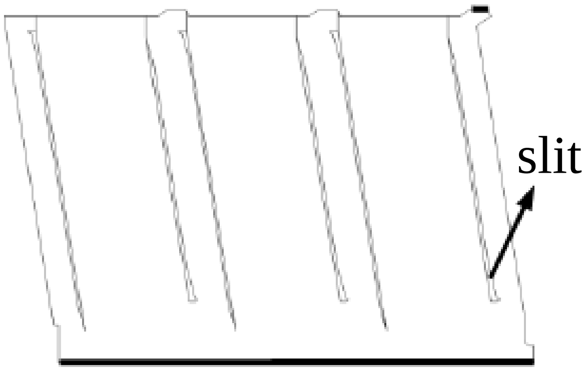
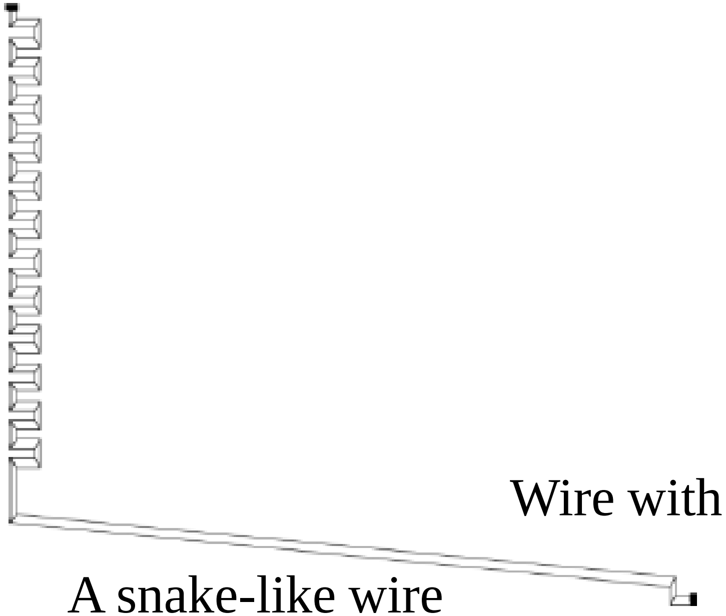
Wire Resistance Calculation

- Structure characteristics
  - ☐ Narrow routing area and equal-resistance object make wires with very complex geometry
  - ☐ Since planar manufactory technology is employed, the wire geometry can often be regarded as a 2-D structure



Structure with slits



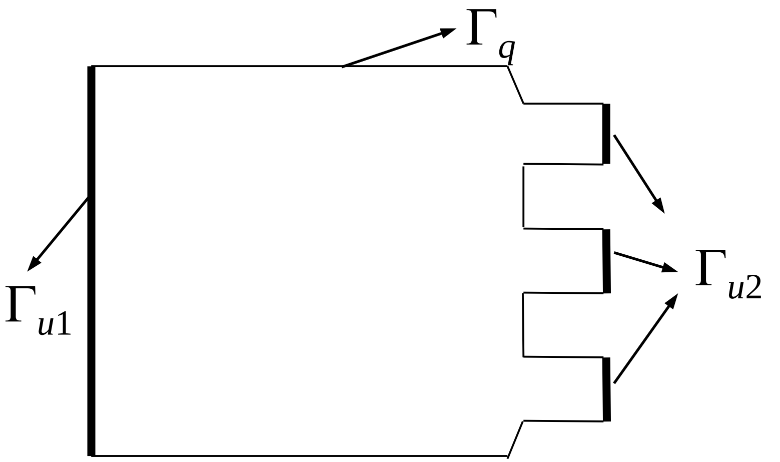
Wire with multi-edge port

A snake-like wire

  - ☐ Call for field solver!

Wire Resistance Calculation

- 2-D boundary element method



Electric potential $u(\boldsymbol{r})$ fulfills:

$$\nabla^2 u(\boldsymbol{r}) = \frac{\partial^2 u(\boldsymbol{r})}{\partial x^2} + \frac{\partial^2 u(\boldsymbol{r})}{\partial y^2} = 0$$

and boundary conditions:

$$\begin{cases} u(\boldsymbol{r}) = u_0, & \text{at } \Gamma_{u1} \text{ or } \Gamma_{u2} \\ \dfrac{\partial u(\boldsymbol{r})}{\partial \vec{\boldsymbol{n}}} = 0, & \text{at } \Gamma_q \end{cases}$$

Resistance

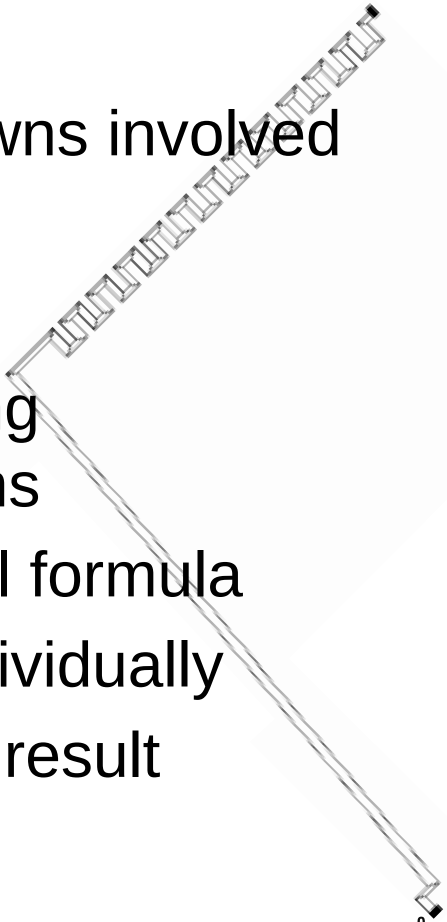
$$\Rightarrow \quad R = \frac{V_1 - V_2}{I} = \frac{1}{I} = \left(\int_{\Gamma_{u1}} \sigma \underbrace{\frac{\partial u(\boldsymbol{r})}{\partial \vec{\boldsymbol{n}}}}_{q} d\boldsymbol{r} \right)^{-1}$$

  - Discretize boundary Γ into *N* elements (segments)
  - Direct BIE $\frac{1}{2} u_k = \sum_{j=1}^{N} q_j \int_{\Gamma_j} u_k^*(\boldsymbol{r}) d\boldsymbol{r} - \sum_{j=1}^{N} u_j \int_{\Gamma_j} q_k^*(\boldsymbol{r}) d\boldsymbol{r}, \quad k = 1, \cdots, N$

    $u_k^*(\boldsymbol{r})$ and $q_k^*(\boldsymbol{r})$ are two known Green's functions $\Rightarrow$ $\boldsymbol{Ax} = \boldsymbol{b}$
  - $\boldsymbol{x}$ consists of $\boldsymbol{q}$ unknowns and $\boldsymbol{u}$ unknowns

Wire Resistance Calculation

- 2-D boundary element method
  - With an automatic boundary partition approach, it works well for some small structures
  - For the long-wire structure, a lot of unknowns involved
- An analytical-BEM coupled approach
  - Follows the divide-and-conquer idea
  - Divide the wire into some portions with long rectangle shape and the remaining portions
  - The rectangle part is solved with analytical formula
  - The remain parts are solved with BEM individually
  - Their results are combined to get the final result



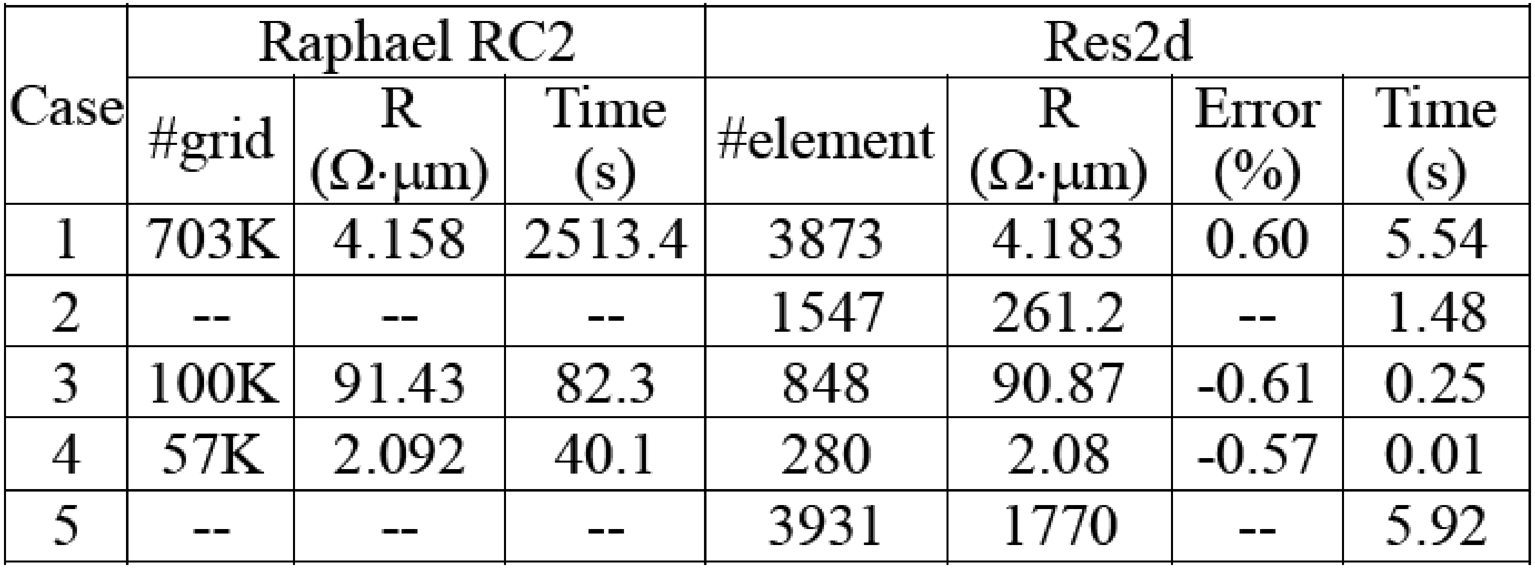
Wire Resistance Calculation

Algorithm 1: The analytical-BEM coupled approach

```
R := 0;
Calculate the tilt angle $\theta_i$, ($i$=1, ..., $n$) of all outer-loop edges
  of the wire profile;
For $i$=1,…,$n$     //$n$ is the number of outer-loop vertices
  For $j$=$i$+1,…,$n$
    If $|\theta_i - \theta_i| < \theta_{tol}$, then
      Calculate the valid rectangle;
      If there is a rectangle with length/width ratio> $\eta$, then
        Obtain a long-wire rectangle by cutting length of 3X
        width from the both ends of the valid rectangle;
        Calculate resistance $R_{rec}$ of the long-wire rectangle;
        $R := R + R_{rec}$;
        Cut off the long-wire rectangle, and adjust ports;
      Endif
    Endif
  Endfor
Endfor
For each left portion of the wire,
  Use BEM to calculate resistance $R_{lef}$;
  $R := R + R_{lef}$;
EndFor
```

Wire Resistance Calculation

- Numerical results of *Res2d*
  - ☐ Use LAPACK to solve Ax=b in BEM
  - ☐ Experiments on a Linux server with Xeon 6-core CPU
  - ☐ Several FPD wires are calculated (assuming $\sigma=1$)
  - ☐ Results compared with Raphael RC2 (golden tool)

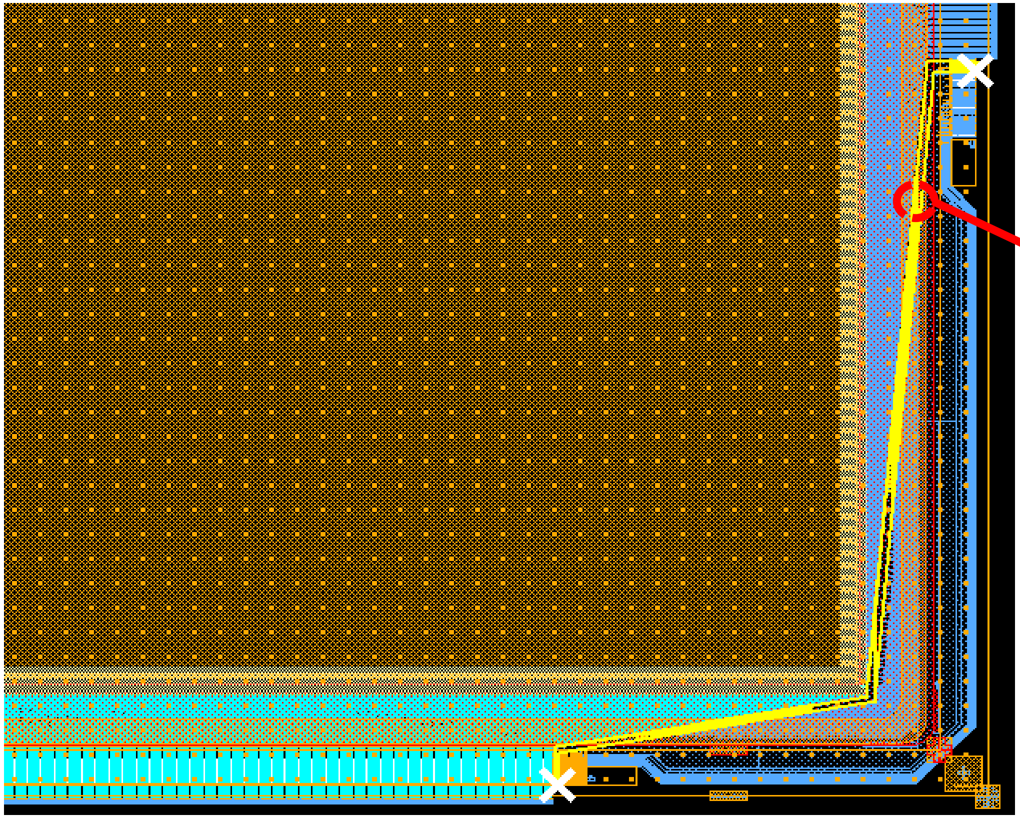


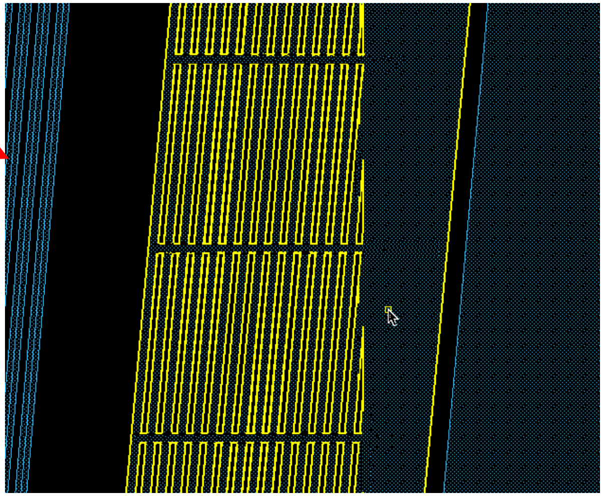
Case	Raphael RC2			Res2d			
	#grid	R (Ω·μm)	Time (s)	#element	R (Ω·μm)	Error (%)	Time (s)
1	703K	4.158	2513.4	3873	4.183	0.60	5.54
2	--	--	--	1547	261.2	--	1.48
3	100K	91.43	82.3	848	90.87	-0.61	0.25
4	57K	2.092	40.1	280	2.08	-0.57	0.01
5	--	--	--	3931	1770	--	5.92

300X~400X Faster!

Wire Resistance Calculation

- Numerical results of *Res2d* (a real design)





both straight segments and slits

Res2d costs 15.3 seconds to calculate the resistance. The result is 18.138 Ω, which well matches the result from a third-party solver based on FEM.

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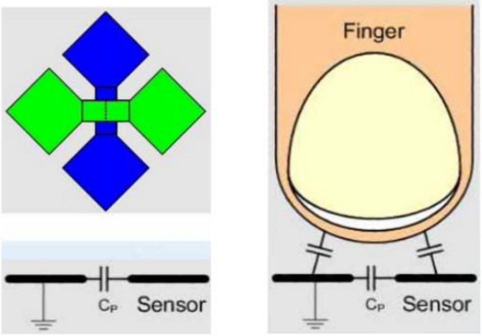
TP-FPD Capacitance Calculation



- Structure complexity
  - Touch sensor, FPD wires, finger stylus
  - Calls for 3-D field-solver solution
- Methods for 3-D capacitance solver
  - Finite difference/finite element method
    - Stable, versatile; slow
  - Boundary element method
    - Fast, handle complex geometry
    - Not scalable, need discretization (may affect accuracy)
  - Floating random walk method
    - Scalable for large problem (low memory cost)
    - No discretization of problem domain (stable accuracy)

$$\left.\begin{matrix}\\ \\ \\ \end{matrix}\right\} Ax = b$$

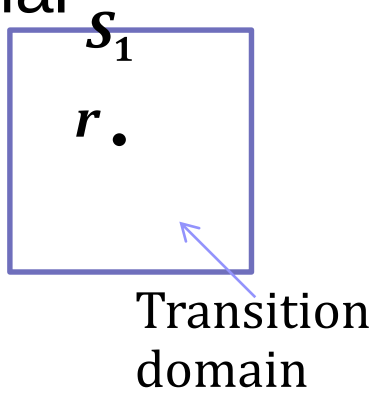
Raphael, Q3D

FastCap, Act3D
QBEM/HBBEM

QuickCap/Rapid3D, RWCap

TP-FPD Capacitance Calculation

- The basics of FRW method
  - Integral formula for the electrostatic potential



$$\phi(\boldsymbol{r}) = \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)})\phi(\boldsymbol{r}^{(1)})ds^{(1)}$$

P_1 is called surface Green’s function, and can be regarded as a probability density function

  - Monte Carlo method: $\phi(\boldsymbol{r}) = \dfrac{1}{M}\sum_{m=1}^{M}\phi_m$

ϕ_m is the potential of a point on S_1, randomly sampled with P_1

  - What if ϕ_m is unknown? expand the integral recursively

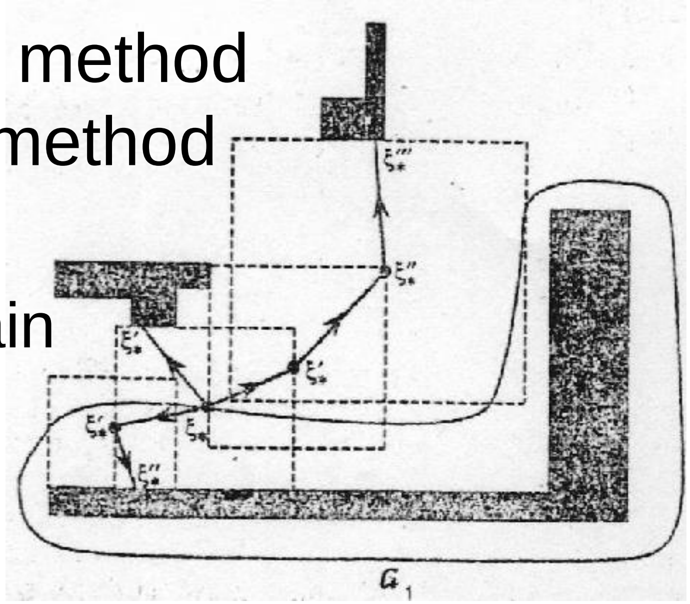
$$\phi(\boldsymbol{r}) = \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)})\oint_{S_2} P_1(\boldsymbol{r}^{(1)}, \boldsymbol{r}^{(2)})\cdots$$

$$\oint_{S_k} P_1(\boldsymbol{r}^{(k-1)}, \boldsymbol{r}^{(k)})\phi(\boldsymbol{r}^{(k)})ds^{(k)}\cdots ds^{(2)}ds^{(1)}$$

This spatial sampling procedure is called **floating random walk**

TP-FPD Capacitance Calculation

- The Markov random process + MC method prove the correctness of the FRW method
- A 2-D example with 3 walks
  - ☐ Use maximal cubic transition domain
- How to calculate capacitances?



Definition: $$\begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{12} & C_{22} & C_{23} \\ C_{13} & C_{23} & C_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \end{bmatrix}$$

$$\boldsymbol{Q_1 = C_{11} V_1 + C_{12} V_2 + C_{13} V_3}$$

Integral for calculating charge (Gauss theorem)

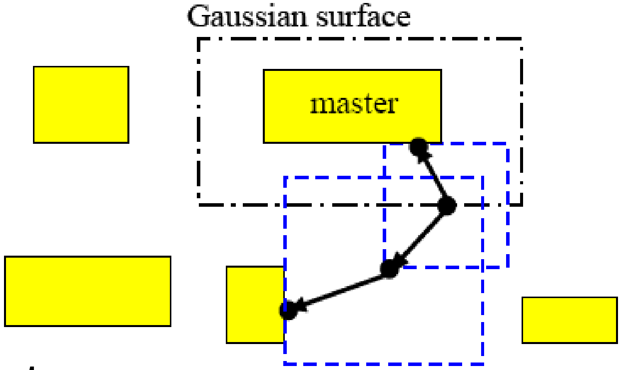
$$Q_1 = \oint_{G_1} F(\boldsymbol{r}) \cdot \hat{n} \cdot \nabla \phi(\boldsymbol{r}) d\boldsymbol{r} = \oint_{G_1} F(\boldsymbol{r}) \cdot \hat{n} \cdot \nabla \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)}) \phi(\boldsymbol{r}^{(1)}) ds^{(1)} ds$$

$$= \oint_{G_1} F(\boldsymbol{r}) g \oint_{S_1} P_1(\boldsymbol{r}, \boldsymbol{r}^{(1)}) \phi(\boldsymbol{r}^{(1)}) \boxed{\omega(\boldsymbol{r}, \boldsymbol{r}^{(1)})} ds^{(1)} ds$$

weight value, estimate of C_{11}, C_{12}, C_{13} coefficients

TP-FPD Capacitance Calculation

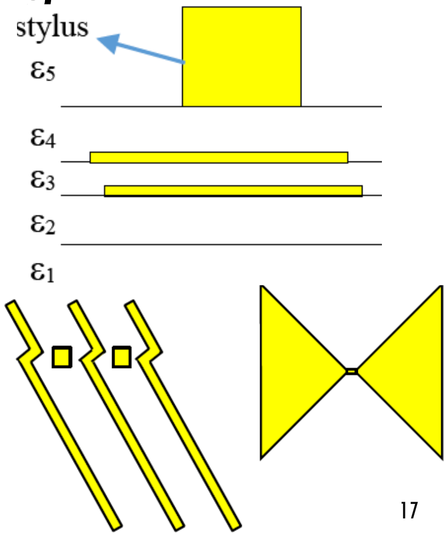
- The secrets of fast FRW solver for VLSI interconnects
  - ☐ Cubic transition domain fits geometry
  - ☐ Numerically pre-calculate transition probabilities and weight values
  - ☐ Importance sampling; placement of Gaussian surface; space management



- Differences in VLSI design & TP-FPD design

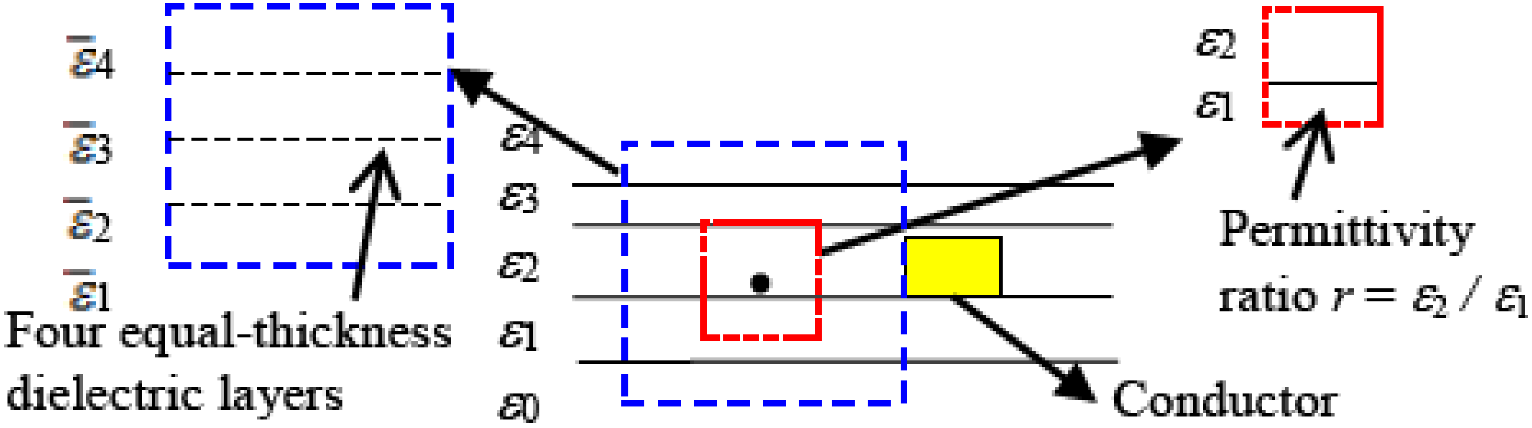
Cap. Extract. for VLSI vs. Cap. Simul. for TP-FPD

Conductor geometry	Mostly Manhattan shape, with moderate aspect ratio	Generally non-Manhattan shape, with very large aspect ratio
Dielectric environment	On-chip dielectric insulators; relatively fixed dielectric profile	In-device dielectrics and out-device air; arbitrary dielectric configuration
Accuracy demand	Mainly self-capacitance for delay calculation	Need accurate coupling capacitances



TP-FPD Capacitance Calculation

- Proposed techniques
  - Geometry engine for non-Manhattan metal shape, which allows planar rotation of transition cube
  - A unified dielectric pre-characterization approach
    - Dielectric homogenization or a new approach?

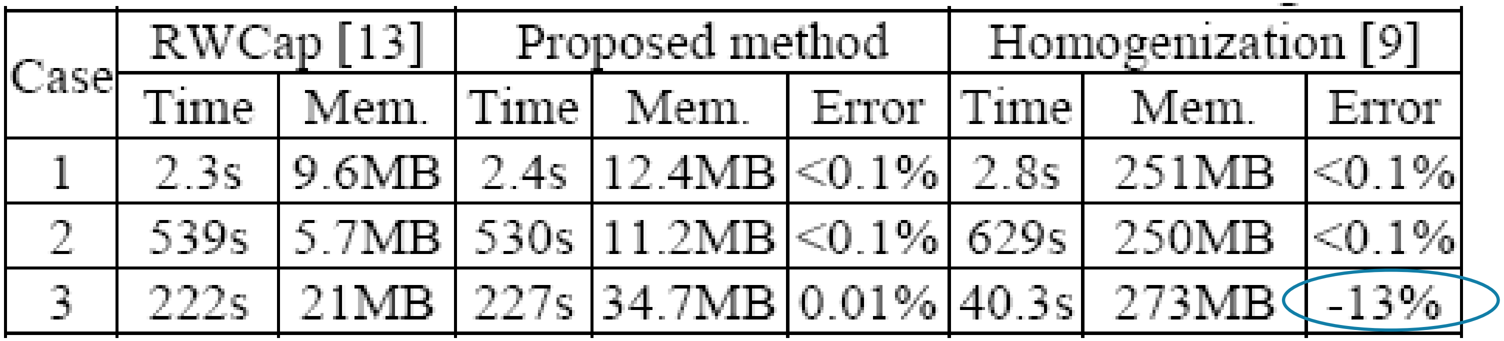


Works only if the permittivity ratio ≤ 2, and Has larger error

Pre-characterize the two-dielectric configurations with $0.1 \le r < 1$; Allows permittivity ratio up to 10 !

TP-FPD Capacitance Calculation

- Proposed techniques
  - ☐ A unified dielectric pre-characterization approach
    - ☐ Experimental results with 3 TP-FPD structures
    - ☐ Dielectric permittivity ranges from 1.0 to 7.0



Case	RWCap [13]		Proposed method			Homogenization [9]		
	Time	Mem.	Time	Mem.	Error	Time	Mem.	Error
1	2.3s	9.6MB	2.4s	12.4MB	<0.1%	2.8s	251MB	<0.1%
2	539s	5.7MB	530s	11.2MB	<0.1%	629s	250MB	<0.1%
3	222s	21MB	227s	34.7MB	0.01%	40.3s	273MB	-13%

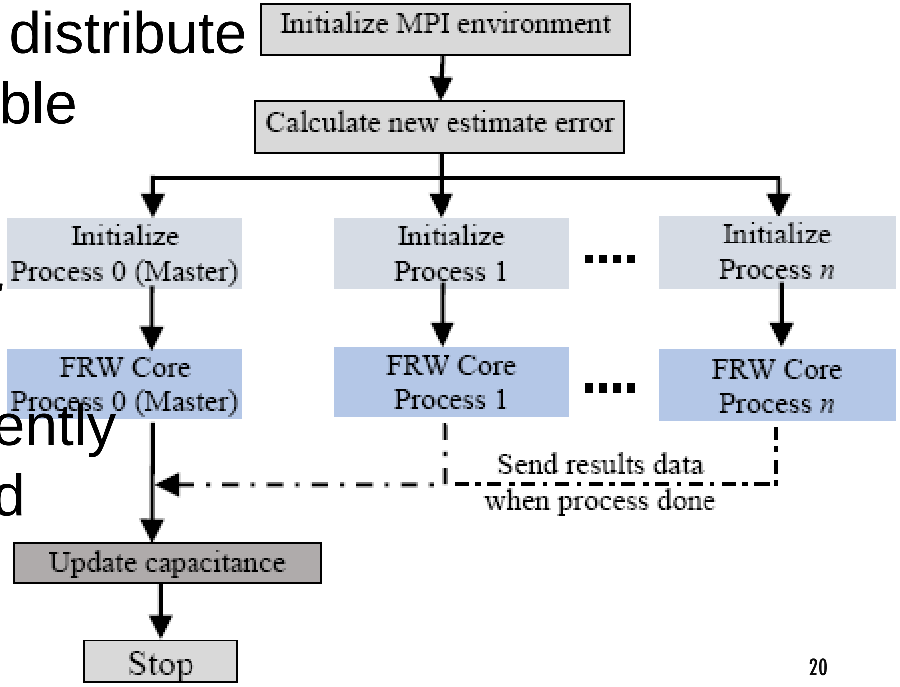
- ☐ Homogenization approach with modification has large error
- ☐ The new approach is accurate and consumes less memory
- ☐ With only 177MB pre-characterization data, it suits to any dielectric profile of TP-FPD technology

TP-FPD Capacitance Calculation

- Proposed techniques
  - Parallel simulation on a computer cluster
    - For accurately calculating the coupling capacitances, further acceleration is necessary
    - Develop a parallel FRW algorithm for distributed computing
    - To minimize communication, distribute the task through setting suitable termination criterion

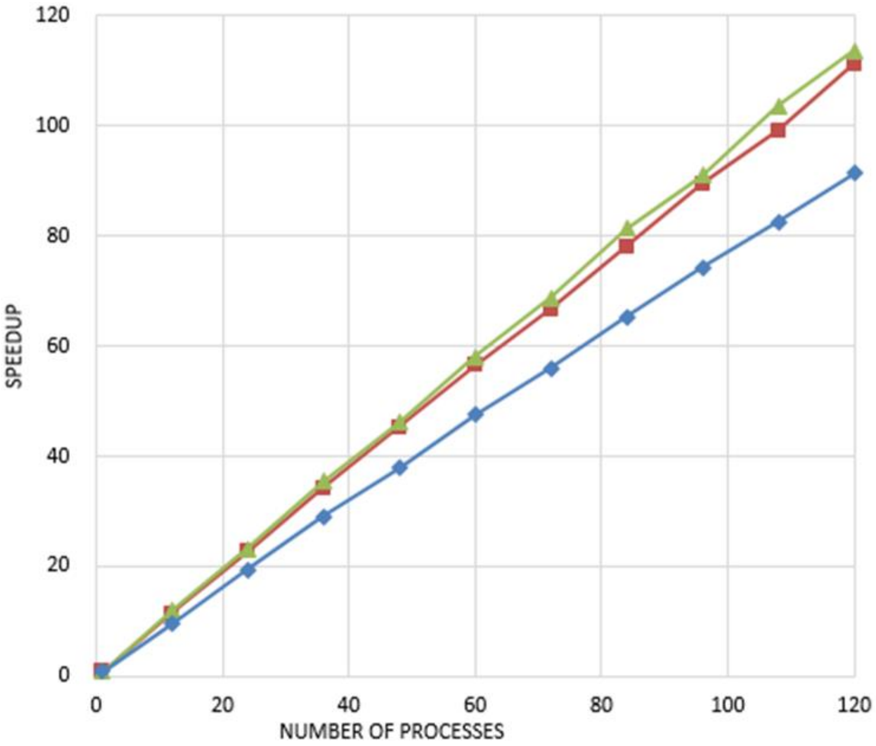
$$err \propto \frac{1}{\sqrt{N_{walk}}} \Rightarrow err' = \sqrt{n_{proc}} \cdot err$$

    - Each process runs independently until its termination is reached



TP-FPD Capacitance Calculation

- Proposed techniques
  - ☐ Parallel simulation on a computer cluster
    - ☐ Implemented with MPI on a homogenous cluster
    - ☐ Three test cases are run with 0.1% 1-σ error



With 120 processes, the speedup is 91X, 111X and 113X

Notice in our previous work [GLSVLSI'2016], the speedup is at most 67X, under same settings

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Conclusions

- Efficient resistance/capacitance calculation techniques have been developed for the design of high-quality FPD and TP-FPD

- The applications in Empyrean CAD toolset validated their effectiveness and practicality

- They have brought benefits to the time-to-market and yield of FPD products

Thank You !

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