Shan Shen

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BASIC INFO.

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EDUCATION

Southeast University — Nanjing, China
Ph.D. candidate, School of Electronic Science & Engineering — *Sep. 2016 – present*
- Supervisor: Prof. Longxing Shi
- Dissertation Title: Performance Modeling And Evaluation of Timing Speculative SRAM

Jiangnan University — Wuxi, China
B.S., School of Internet of Things Engineering — *Sep. 2012 – July 2016*

RESEARCH INTERESTS

1. Circuit Modeling And Optimization
Large capacity SRAM design requires high σ yield evaluation, which is the most time-consuming process in the customized design flow. My research aims at finding a fast and accurate method to estimate the performance and yield of large-scale memory circuits.

2. Low-Power Circuit And Architecture Design
To mitigate the ever-worsening "Power Wall" problem, more and more SoC devices need to expand their working voltage to the wide-voltage range including the near-threshold region. We have proposed several techniques from both circuit and architectural levels to boost the frequency and improve the energy efficiency of on-chip memory.

PUBLICATIONS

[1] **Shen, Shan**, Liang Pang, Tianxiang Shao, Ming Ling, Xiao Shi, and Longxing Shi. "TYMER: a yield-based performance model for timing-speculation SRAM." In *2020 57th ACM/IEEE Design Automation Conference (DAC)*, pp. 1-6. IEEE, 2020.
[2] **Shen, Shan**, Tianxiang Shao, Ming Ling, Jun Yang, and Longxing Shi. "Modeling and designing of a PVT auto-tracking timing-speculative SRAM." In *2020 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 1073-1078. IEEE, 2020.
[3] **Shen, Shan**, Tianxiang Shao, Xiaojing Shang, Yichen Guo, Ming Ling, Jun Yang, and Longxing Shi. "TS cache: A fast cache with timing-speculation mechanism under low supply voltages." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 28, no. 1 (2019): 252-262.
[4] **Shen, Shan**, Ming Ling, Yongtao Zhang, and Longxing Shi. "Detecting the phase behavior on cache performance using the reuse distance vectors." *Journal of Systems Architecture* 90 (2018): 85-93.
[5] **Shen, Shan**, et al. "A Timing Yield Model for SRAM in Sub/Near-threshold Voltages Based on A Compact Drain Current Model", TCAD, in submission.

Other papers as a co-author:
[6] Ling, Ming, Qingde Lin, Ke Tan, Tianxiang Shao, **Shan Shen**, and Jun Yang. "A Design of Timing Speculation SRAM-Based L1 Caches With PVT Autotracking Under Near-Threshold Voltages." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 01 (2021): 1-13.
[7] Pang, Liang, **Shan Shen**, and Mengyun Yao. "A Spline-High Dimensional Model Representation for SRAM Yield Estimation in High Sigma and High Dimensional Scenarios." *IEEE Access* 9 (2021): 47320-47329.
[8] Shang, Xiaojing, Ming Ling, **Shan Shen**, Tianxiang Shao, and Jun Yang. "RRS cache: a low voltage cache based on timing speculation SRAM with a reuse-aware cacheline remapping mechanism." In *Proceedings of the International Symposium on Memory Systems*, pp. 451-458. 2019.
[9] Ling, Ming, Xiaojing Shang, **Shan Shen**, Tianxiang Shao, and Jun Yang. "Lowering the hit latencies of low voltage caches based on the cross-sensing timing speculation SRAM." *IEEE Access* 7 (2019): 111649-111661.

PROJECT EXPERIENCE

1. Wide-voltage Timing-speculative Cache Circuit And Architecture Optimization — *2019 – present*
Supported by the National Natural Science Foundation of China (NSFC)

2. Research on Statistical Distribution Model for Low-Voltage Chip Design *2018 – present*
Supported by the National Natural Science Foundation of China (NSFC)

3. Analytical Modeling of Multi-core Out-of-Order Processor Storage Architecture for Mobile Computing *2018 – present*
Supported by the Natural Science Foundation of Jiangsu Province

4. Overlay Process Unit *Sep. 2020 – Sep. 2021*
Collaborated with UCLA, EAD Laboratory.

1. OPU is a domain-specific FPGA overlay processor to accelerate CNN networks. I'm in charge of the hardware implementation for natural language processing.

5. Benchmark Reduction Technology Research *2016 – 2017*
Supported by HUAWEI Terminal Department

2. This project is aimed at reducing the Benchmark size in CPU testing to speed up the performance evaluation. I'm in charge of the instruction decoder and the instruction information collection.

SKILLS

1. Digital-analog mixed circuit design
I'm familiar with storage circuits and have experience on tape-out. I also can design hardware with RTL.

2. Programming ability
I have proficient programming ability and can use software languages such as C++, Python, and Matlab.

3. Independent research ability
I have a good understanding of CMOS devices, circuits, FPGAs, computer architecture, and software.