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Analytical Frequency-Dependent Model for Transmission Lines on RF-CMOS Lossy Substrates*

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Abstract: Transmission lines (T-Lines) are widely used in millimeter wave applications on silicon-based complementary metal-oxide semiconductor (CMOS) technology. Accurate modeling of T-lines to capture the related electrical effects has, therefore, become increasingly important. This paper describes a method to model the capacitance and conductance of T-Lines on CMOS multilayer, lossy substrates based on conformal mapping, and region subdivision. Tests show that the line parameters (per unit length) obtained by the method are frequency dependent and very accurate. The method is also suitable for parallel multiconductor interconnect modeling for high frequency circuits.

Key words: transmission lines; frequency dependence; capacitance; radio frequency complementary metal-oxide semiconductor (RF-CMOS); circuit characteristics

Introduction

In the past, III/V compound technologies were the only choice for millimeter wave applications. As the feature size of complementary metal-oxide semiconductor (CMOS) technologies have become smaller, the speed gap between III/V and silicon based technologies has been significantly decreased. Thus, more and more designers are trying to implement monolithic microwave integrated circuits (MMIC) on silicon substrates[1-3].

In microwave integrated circuits, transmission lines (T-Lines) are important structures for matching networks and resonators. At millimeter wave frequencies, the required inductances are of the order of 50-250 pH[2]. Only T-Lines are capable of resizing precisely at such small values. Another benefit of using T-Lines is that the well-defined ground return path significantly reduces magnetic and electric field coupling to adjacent structures.

Most previous studies have focused on T-Lines on lossless dielectrics, and the frequency dependence due to the dielectric conductivity has seldom been addressed. Unlike T-Lines implemented on GaAs, where the conductance is essentially zero and the capacitance is constant, T-Lines implemented on low-resistivity silicon often have low capacitive quality factors due to the substrate coupling, and both the conductance and the capacitance are frequency dependent.

Previous works[4,5] used conformal mapping techniques to give exact or very accurate solutions for T-Lines in homogeneous dielectric. The validity of conformal mapping for T-Line analysis relies on the assumption that the propagation mode in the T-Lines is quasistatic, which is valid up to a frequency of 100 GHz[6].

Chen and Chou[7] used the Veyers-Fouad Hanna approximation for T-Lines in double-layer dielectrics (with superposition of partial capacitances[8]) and extended the analysis to multiple dielectric layers.

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However, this approximation needs the strong assumption that all the boundaries of the dielectrics are along the electric field lines. To be accurate, this assumption requires that for two adjacent dielectric layers, the permittivity of the inner dielectric (the one closer to the T-Line) is larger than that of the outer one, which is valid for differential electro-optic sampling (DEOS), is not valid for CMOS technology.

Sytchev[9] gave the solution for when the Veyers-Fouad Hanna approximation does not hold, that the permittivity of the inner dielectric is smaller than that of the outer layer, and showed it to be valid for a double layer design. However its accuracy for multi-layer dielectrics is unknown. More importantly, none of these works considered the frequency dependent effects reflecting the substrate losses. These two issues will be addressed in this paper.

1 Problem Formulation

Transmission lines in lossy dielectrics can be characterized by the frequency dependent parameters $R(\omega)$, $L(\omega)$, $C(\omega)$, and $G(\omega)$.

Analytical models for the series impedance parameters $R(\omega)$ and $L(\omega)$ in simple dielectrics have been presented in Heinrich[4]. For CMOS devices, all dielectrics are assumed to be non-magnetic and the models for R/L[4] are still valid and are used in this paper. This paper focuses on modeling C/G in multi-layer dielectric and lossy substrates, which with the frequency-dependent R/L model, constitute a complete model for coplanar waveguide (CPW) T-Lines.

The problem configuration is shown in Fig. 1, where the coplanar T-Lines with n conductors, including both signal and ground conductors, are embedded in N dielectric layers. Each dielectric layer has its own thickness t_i, permittivity ε_i, and conductivity σ_i. The bottom of the substrate is assumed to be perfectly grounded. The conductors are laid on the bottom of the m-th layer. The conductive substrate is modeled by a complex permittivity[10]

$$\dot{\varepsilon}_i = \varepsilon_i + \frac{\sigma_i}{\mathrm{j}\omega} \tag{1}$$

which accounts for both ohmic and displacement currents and the frequency dependent effects of the conductive dielectric.

The frequency dependent line parameters of the T-Line are described by a complex matrix $\tilde{\boldsymbol{C}}$ which includes both $\boldsymbol{C}$ and $\boldsymbol{G}$,

$$\tilde{\boldsymbol{C}} = \boldsymbol{C} + \frac{1}{\mathrm{j}\omega}\boldsymbol{G} \tag{2}$$

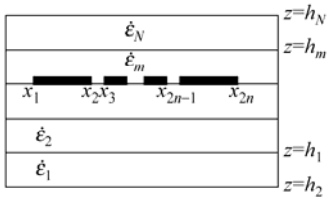

Fig. 1 T-Lines geometry

Each entry in matrix $\tilde{\boldsymbol{C}}$, $\tilde{C}_{ij}$ is defined as the charge on conductor i when a unit voltage is applied on conductor j while all the other conductors are perfectly grounded.

The capacitance $\tilde{\boldsymbol{C}}$ can be divided into three parts[4]

$$\tilde{\boldsymbol{C}} = \tilde{\boldsymbol{C}}^{\text{upper}} + \tilde{\boldsymbol{C}}^{\text{lower}} + \tilde{\boldsymbol{C}}^{\text{sidewall}} \tag{3}$$

where $\tilde{\boldsymbol{C}}^{\text{upper}}$ indicates the contribution of dielectrics above the conductors. Similarly, $\tilde{\boldsymbol{C}}^{\text{lower}}$ indicates the contribution from dielectrics below the conductors. When computing $\tilde{\boldsymbol{C}}^{\text{upper}}$ and $\tilde{\boldsymbol{C}}^{\text{lower}}$, the conductors are assumed to be infinitely thin without sidewalls with the sidewall effect included in $\tilde{\boldsymbol{C}}^{\text{sidewall}}$, which is a tri-diagonal matrix denoting the sidewall coupling between adjacent conductors. The sidewall coupling between non-adjacent conductors is neglected.

The analytical model in Heinrich[4] is accurate for transmission lines between two dielectrics. In CMOS devices, however, the dielectric is a more complicated, multilayered structure as shown in Fig. 1.

For CPWs in multilayered dielectrics, Chen and Chou[7] proposed a superposition approximation method, which is also referred to as the Veyers-Fouad Hanna approximation. This approximation, however, is only exact when all the boundaries of the dielectrics are along the electric field line, and is accurate only when the permittivity of the dielectrics decrease as their distances from the CPWs increase. Thus, the permittivities must satisfy

$$\varepsilon_1 << \varepsilon_2 << \cdots << \varepsilon_m \tag{4}$$

$$\varepsilon_m >> \varepsilon_{m+1} >> \cdots >> \varepsilon_N \tag{5}$$

Inequalities (4) and (5) hold quite well for the DEOS configuration[7], but are not satisfied in typical CMOS technologies. CMOS technologies have metal in the oxide layers with a permittivity of 3.9 and the

permittivity of the silicon substrate is 11.9, which violates Inequality (4). Therefore, the superposition approximation[7] is not suitable for CMOS devices. Hence, the Veyers-Fouad Hanna approximation is combined with the Sytchev approximation[9] in a recursive procedure.

The procedure starts from $\tilde{\boldsymbol{C}}^{\text{lower}}$. Suppose the contributions of layers 1 to k sum to $\tilde{\boldsymbol{C}}_k^{\text{lower}}$, then $\tilde{\boldsymbol{C}}_k^{\text{lower}}$ is a combination of $\tilde{\boldsymbol{C}}_{k-1}^{\text{lower}}$ and $\tilde{\boldsymbol{C}}_x(\boldsymbol{x}, h_m - h_k)$, where $\tilde{\boldsymbol{C}}_x(\boldsymbol{x}, h_m - h_k)$ is the capacitance of one of the configurations in Fig. 2. The exact solution for Fig. 2a was given by Homentcovschi[5], while the solution for Fig. 2b can be obtained by simple modifications of their results. The recursive procedure is detailed as follows.

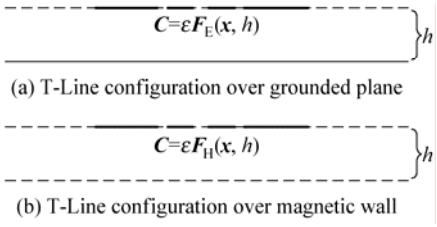

Fig. 2 T-Lines on perfect boundary conditions. Solid lines denote the electric walls and dashed lines denote magnetic walls.

First, since the bottom of the chip is assumed to be perfectly grounded,

$$\tilde{\boldsymbol{C}}_1^{\text{lower}} = \dot{\varepsilon}_1 \boldsymbol{F}_{\text{E}}(\boldsymbol{x}, h_m) \tag{6}$$

where vector $\boldsymbol{x}$ is the conductor coordinates defined in Fig. 1. $\boldsymbol{F}_{\text{E}}(\boldsymbol{x}, h_m)$ is the solution without the permittivity factor for Fig. 2a. Hence, all the dielectrics below the conductors have the same permittivity as layer 1.

If $|\dot{\varepsilon}_k| > |\dot{\varepsilon}_{k-1}|$, the electric field on the layer k side of the interface is approximately parallel to the interface, so the Veyres-Fouad Hanna approximation[8] can be adopted,

$$\tilde{\boldsymbol{C}}_k^{\text{lower}} = \tilde{\boldsymbol{C}}_{k-1}^{\text{lower}} + \tilde{\boldsymbol{C}}_{\text{H},k} \tag{7}$$

where

$$\tilde{\boldsymbol{C}}_{\text{H},k} = (\dot{\varepsilon}_k - \dot{\varepsilon}_{k-1}) \boldsymbol{F}_{\text{H}}(\boldsymbol{x}, h_m - h_k) \tag{8}$$

where $\boldsymbol{F}_{\text{H}}(\boldsymbol{x}, h_m - h_k)$ is the solution for conductors over a perfect magnetic wall as shown in Fig. 2b. $\tilde{\boldsymbol{C}}_{\text{H},k}$ is actually the capacitance when all the dielectrics between the conductors and the bottom of layer k have the same permittivity $\dot{\varepsilon}_k - \dot{\varepsilon}_{k-1}$, and the bottom of layer k is replaced by a perfect magnetic wall.

The dielectric permittivity of the layers above layer k–1 should then be modified to

$$\dot{\varepsilon}_i = \dot{\varepsilon}_i - \dot{\varepsilon}_{k-1}, \quad k \leqslant i < m \tag{9}$$

so that the contribution of $\dot{\varepsilon}_{k-1}$ will not be accounted for again.

If $|\dot{\varepsilon}_k| < |\dot{\varepsilon}_{k-1}|$, the electric field is approximately perpendicular to the interface, so the Sytchev approximation[9] is adopted,

$$\tilde{\boldsymbol{C}}_k^{\text{lower}} = \left[\left(\tilde{\boldsymbol{C}}_{k-1}^{\text{lower}} \right)^{-1} + \left(\tilde{\boldsymbol{C}}_{\text{E},k} \right)^{-1} \right]^{-1} \tag{10}$$

where

$$\tilde{\boldsymbol{C}}_{\text{E},k} = \left(\frac{\dot{\varepsilon}_k \dot{\varepsilon}_{k-1}}{\dot{\varepsilon}_{k-1} - \dot{\varepsilon}_k} \right) \boldsymbol{F}_{\text{E}}(\boldsymbol{x}, h_m - h_k) \tag{11}$$

Similarly, the dielectric permittivity of the layers above layer k–1 should then be modified as

$$\dot{\varepsilon}_i = \frac{1}{1/\dot{\varepsilon}_i - 1/\dot{\varepsilon}_{k-1}}, \quad k \leqslant i < m \tag{12}$$

Finally, $\tilde{\boldsymbol{C}}^{\text{lower}}$ is given by

$$\tilde{\boldsymbol{C}}^{\text{lower}} = \tilde{\boldsymbol{C}}_m^{\text{lower}} \tag{13}$$

Similarly, $\tilde{\boldsymbol{C}}^{\text{upper}}$ is obtained using almost the same method from the top layer downwards. The only difference is that the top plate of the conductor is insulated rather than perfectly grounded as on the bottom one.

The sidewall capacitance $\tilde{\boldsymbol{C}}^{\text{sidewall}}$ can be given directly using the formula from Heinrich[4],

$$\tilde{C}_{i,i\pm1}^{\text{sidewall}} = -\dot{\varepsilon}_m p_{c0} \left[\frac{t}{s} \left(p_{c1} - \ln \frac{2t}{s} \right) + \left(\frac{t}{s} \right)^2 \left(1 - \frac{3}{2} p_{c2} + p_{c2} \ln \frac{2t}{s} \right) \right] \tag{14}$$

where t and s are the conductor thickness and spacing. The coefficients p_{c0}, p_{c1}, and p_{c2} were given by Heinrich[4].

2 Results

2.1 Two signal conductor T-Line

A T-Line with two signal conductors over a radio frequency (RF) CMOS substrate was used to evaluate the capacitance calculation method. A design for a common RF CMOS technology is shown in Fig. 3a. The T-Line has two signal conductors with two ground conductors on both sides as shown in Fig. 3b.

Since the 4 conductors include only two ground

conductors, the computed 4×4 capacitance matrix $\tilde{\boldsymbol{C}}$ is reduced to a 2×2 matrix. The complex capacitance is then converted to a real capacitance and conductance by

$$\boldsymbol{C} = \mathrm{Re}[\tilde{\boldsymbol{C}}], \quad \boldsymbol{G} = -\omega\,\mathrm{Im}[\tilde{\boldsymbol{C}}].$$

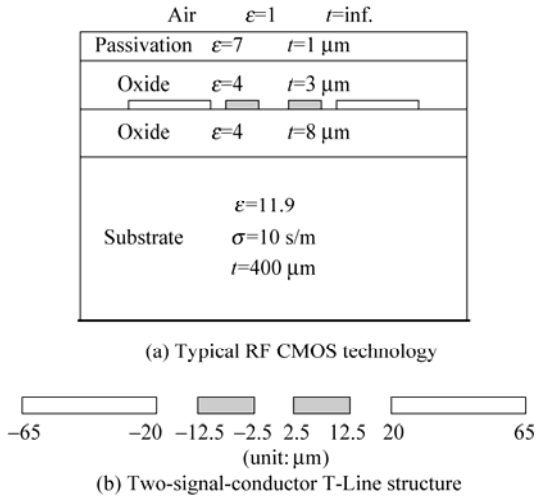

Fig. 3 A T-Line structure with two signal conductors over substrate. The hollow blocks are the ground conductors, and the solid blocks are the signal conductors.

The resulting $\boldsymbol{C}$ and $\boldsymbol{G}$ are compared with a special 2-D version of the quasi-static electric-magnetic (EM) solver SCAPE[11], whose accuracy has been well verified by comparison with commercial EM solvers, in Figs. 4 and 5. The method presented by Chen and Chou[7] is also presented as a reference.

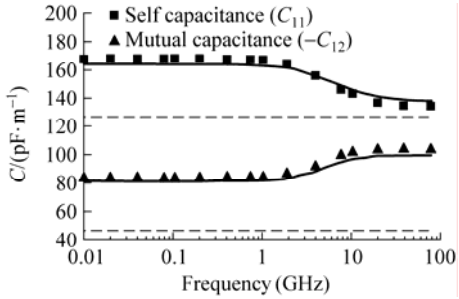

Fig. 4 Capacitance for two-signal-conductor transmission line. The symbols are the EM simulation results. The solid lines are the present results. The dashed lines show the results of Chen and Chou[7].

The present analytical results agree well with the previous models. The complex capacitance predicted by the current method is within 2% of the EM solver result. The result given by Chen and Chou[7] gives frequency independent capacitance and conductance, with quite a large error compared to the EM result.

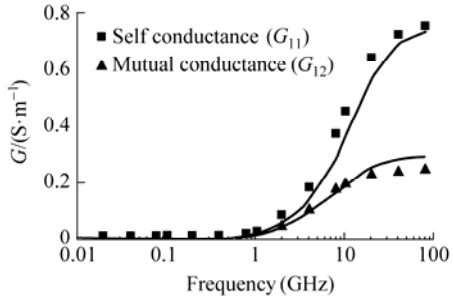

Fig. 5 Conductance for two-conductor T-Line. The symbols are the EM simulation results. The solid lines are the present results.

In terms of efficiency, the present analytical results used 16 frequency points with less than 1/10 of CPU time on a P4 2.8-GHz CPU, which is much faster than the numerical EM solver.

2.2 Frequency domain simulation of CPW

The present capacitance calculation can be combined with the inductance and resistance formula[4] to simulate the overall performance of CPWs.

The design is the same as in Fig. 3, with the CPW structure and parameters given in Fig. 6a. The results are compared with those of momentum in the Agilient ADS which is a full-wave EM solver for microwave and RF circuit simulations.

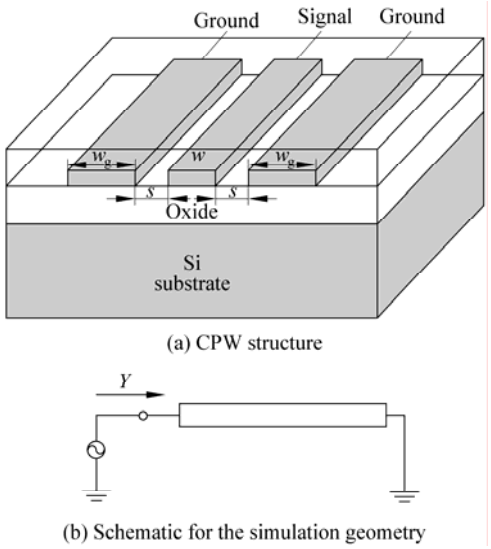

Fig. 6 A CPW structure for simulation of capacitance, resistance, and inductance

In this test case, the ground line width is fixed at $w_g = 200$ μm with spacings $s = 10$ μm and a CPW length of 1000 μm.

For simplicity, the far end of the CPW is assumed to be shorted to the ground, with the *Y*-parameter (i.e., $j\omega\tilde{\boldsymbol{C}}$) of the near end compared in Fig. 6b.

The results for different line widths is shown in Fig. 7, with the errors plotted in Fig. 8. The present analytical formulas agree well with the EM simulation results with errors typically less than 5% up to 20 GHz.

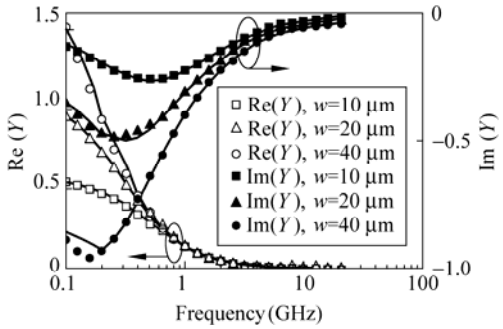

Fig. 7 *Y*-parameters for the CPW in Fig. 6. The symbols represent the EM simulation results using Momentum and the solid lines are the present results.

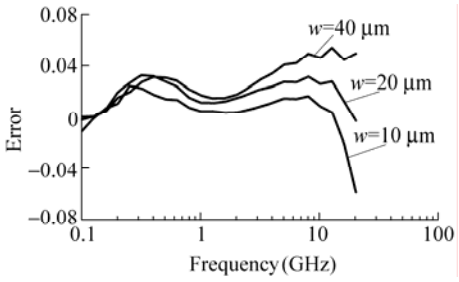

Fig. 8 Errors of the *Y*-parameters for the CPW in Fig. 6

3 Conclusions

A fully analytical and scalable model is presented to calculate the line (per unit length) parameters for multi-conductor T-Lines. The model is suitable for current RF-CMOS devices with multilayer dielectrics and lossy substrates. This analytical method can quickly model complicated structures and can be easily embedded in CAD tools for fast verification or synthesis of integrated circuit designs.

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