

Hierarchical Block Boundary-Element Method (HBBEM): A Fast Field Solver for 3-D Capacitance Extraction

Taotao Lu, Zeyi Wang, and Wenjian Yu

Abstract—As feature size decrease, fast and accurate parasitic capacitance extraction has become increasingly critical for verification and analysis in very large scale integration design. In this paper, a fast hierarchical-block boundary-element method based on the boundary-element method (BEM) is presented for three-dimensional (3-D) capacitance extraction, which can give out the global capacitance matrix directly. It assigns the global computation of 3-D domain into local computation in BEM blocks by hierarchical partition 3-D structure. The boundary capacitance matrix (BCM) is computed in the BEM block using all the known conditions. Reuse technology can decrease the running time. After merging the BCMS of all BEM blocks, the global capacitance matrix for a given set of conductors can be computed. Numerical results show that this global hierarchical approach can get very high speed in 3-D computation with equal accuracy as the 3-D field solver.

Index Terms—Boundary-element method (BEM), capacitance extraction, hierarchical, very large scale integration (VLSI).

I. INTRODUCTION

AS THE feature size has decreased very quickly, the interconnect is becoming a dominant factor in system delay and signal integrity [12]. For timing verification, accurate interconnect modeling is desired. Parasitic parameter extraction is the most critical step of interconnect modeling. Timing verification needs parasitic parameter extraction to be fast and accurate, especially for the parasitic capacitance extraction.

Currently, none of the fast extraction tools can guarantee high accuracy in capacitance. They use the two-dimensional (2-D) or quasi-three-dimensional (3-D) model to compute the capacitance based on the geometrical characteristics of the interconnects [7], [10], [13]. These methods are fast, but inaccurate, especially for the coupling capacitance as the interconnect structures become more and more complex.

In order to get high accuracy, the numerical methods are often used to solve the field equations, which are called the field solvers. They can be classified as two kinds: the local and global ones. The local approaches are well-known flat field solutions

that solve the Laplace equation with a preset bias on conductors by using the finite-difference method (FDM) [5], finite-element method (FEM) [2] or boundary-element method (BEM) [6], [21], [24], [25], etc. [15], [17], [18], [23]. Many acceleration methods have been presented, such as the multipole acceleration [6], hierarchical acceleration [21], and quasi-multiple medium (QMM) [25]. The method presented by Yu *et al.* [25] can deal with the actual 3-D geometry using the 3-D domain partition to make the QMM acceleration. However, such methods only get one column of a whole capacitance matrix, including all the self-capacitance and coupling capacitance among all the simulated conductors. They are classified as the local methods. If all the coupling capacitance needs to be known, the flat field solution must be repeated for different preset biases many times.

The other kinds of methods are also based on the field solution, but they will not solve the resulting linear system in the usual way. They find the resistance and capacitance without actually looking for the potential distribution. Instead, discretization of the field equations with the FDM or BEM can be represented by a circuit network with resistors or capacitors. After fast reduction of the network, the whole resistance or capacitance matrix can be obtained directly, and they are referred to as the global methods. These approaches have been successfully used for extracting 2-D interconnect resistance [4], [8] or capacitance [1], [8], [20], [14], [19]. In the 1990s, with wide use of the BEM in parasitic extractions, these kinds of methods were further improved to fit the network representation and its reduction from discretization of the boundary elements. The BEM macromodels [19], [20] and dimension-reduction technique (DRT) [22] proposed some valuable ideas such as hierarchical extraction, etc. Though [19] and [20] mentioned the 3-D implications of the hierarchical macromodel extraction, we have not learned 3-D implementation based on the methods of [19] and [20] to date. Besides, the DRT proposed in [22] focuses on the stratified structures, which are limited to regular geometry in 3-D.

There are many difficulties with using the global approach in extracting capacitance of the 3-D structures, such as the huge computational size, high complexity for network reduction, and hierarchical partition of the 3-D structure.

In this paper, a rapid hierarchical global approach to extracting the 3-D interconnect capacitance is presented based on the idea of the hierarchical boundary-element macromodels [19], [20], which can overcome these difficulties in 3-D computation. The capacitance computation is based on the Laplace equation. In our method, the global computation in the 3-D domain is changed into local computation in rectangular

Manuscript received January 17, 2003; revised March 31, 2003. This work was supported by the China National Science Foundation under Grant 69876024, by the China National Foundation for Key Basic Research under Grant G1998030404, and by the China Development Project for Advanced Technology under Grant 2002AA121460SOC.

The authors are with the Electronic Design Automation, Laboratory, Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China.

Digital Object Identifier 10.1109/TMTT.2003.821228

3-D BEM blocks, which are obtained by partition of the 3-D structure. Such a division can be generated by partitioning the 2-D polygon geometry of interconnects and process technology separately. All BEM blocks are organized into one hierarchical tree. In local computation, a matrix called the boundary capacitance matrix (BCM) is computed based on the BEM where all the known conditions are used. Only a few unknown variables are left. Merging all the BCMs of each BEM block can then eliminate all the unknown variables. Through such a process, local matrices are finally merged into a global one. Such a global matrix is the required global capacitance matrix. The local computation can be fast because of its small region. The reuse technology can be used in local computation with the hierarchical approach. Since only a few unknown variables are left in merging process, such an approach is in high speed.

There are three marked features in the approach presented here as follows:

- 1) high speed for the 3-D global capacitance matrix extraction;
- 2) high accuracy based on the 3-D field solution of the BEM;
- 3) obtaining the global solution, i.e., a complete capacitance matrix including all the self-capacitance and coupling capacitance among the simulated conductors.

The remainder of this paper is organized as follows. In Section II, a basic introduction of the 3-D capacitance computation is given. In Section III, the BCM is presented as the basis of our fast hierarchical approach. The basic computations of such a kind of matrix are also presented. In Section IV, the hierarchical computation approach for 3-D capacitance extraction, called the hierarchical-block boundary-element method (HBBEM), is presented, including the complexity analysis and some discussion on gridding. Some numerical results and analysis are listed in Section V. Finally a conclusion is presented in Section VI.

II. 3-D INTERCONNECT CAPACITANCE COMPUTATION

Both the local and global methods solve the Laplace equation with mixed boundary conditions as shown in (1) when computing the capacitance. In the 3-D domain with multiple dielectrics $\Omega = \cup^M \Omega_k$, ($k = 1, \dots, M$), the electrical potential distribution is governed by the Laplace equations

$$\begin{cases} \varepsilon_k \nabla^2 u = \varepsilon_k \left(\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2} \right) = 0 \text{ in } \Omega_k \\ k = 1, \dots, M \\ \varepsilon_a \cdot \frac{\partial u_a}{\partial \mathbf{n}_a} = -\varepsilon_b \cdot \frac{\partial u_b}{\partial \mathbf{n}_b} \quad u_a = u_b \text{ on } \Gamma_I \end{cases} \quad (1)$$

where u is the potential distribution in the domain, $(\partial u_a)/(\partial \mathbf{n}_a)$ is the normal derivative of the potential on the boundary, \mathbf{n}_a is the outer normal on the interface between Ω_a and Ω_b , and ε_k is the permittivity of the domain Ω_k .

The interface boundary condition [(IBC) on Γ_I] is applied in the interface of two dielectrics.

In the local method, the boundary condition should also be applied: the Dirichlet boundary condition [(DBC) on Γ_u] and

Neumann boundary condition [(NBC) on Γ_q], shown in (2) and (3) as follows:

$$u = \bar{u} \text{ on } \Gamma_u \quad (2)$$

$$q = \frac{\partial u}{\partial \mathbf{n}} = \bar{q} = 0 \text{ on } \Gamma_q \quad (3)$$

where \bar{u} is the preset potential on boundary Γ_u and \bar{q} is usually zero on boundary Γ_q .

Using different numerical methods, such as the FDM, FEM, BEM, etc., a linear system can be obtained as follows:

$$Ax = b \quad (4)$$

where vector x contains all the unknown variables.

The coupling capacitance C_{ij} between conductor i and j is

$$C_{ij} = -Q_i/V_{ji} \quad (5)$$

where V_{ji} is the voltage between conductors j and i , and Q_i is the induced charge of conductor i , which can be obtained from

$$Q_i = \int_{\Gamma_i} \varepsilon \cdot q d\Gamma \quad (6)$$

where Γ_i is the surface of conductor i , ε is the dielectric's permittivity, and $q = \partial u / \partial \mathbf{n}$ is the normal derivative of electrical potential along normal \mathbf{n} on Γ_i . q can be solved in (4).

In the global method, (1) can be turned into such a kind of formula $CU = Q$ by different numerical methods, which is different from (4). Matrix C stands for the complete network of all the nodes in the 3-D domain [8]. After eliminating the nodes that are not in the conductors, the reduced matrix is the required matrix.

III. BCM

In this section, one kind of matrix, i.e., the BCM, is presented, which corresponds to the complete network. The computation of such a kind of matrix is the base of our hierarchical global method. Based on the BEM, the BCM can be computed in the 3-D domain.

A. Introduction of BCM

In a 3-D domain with n conductors, there is coupling capacitance between every two conductors. If the 3-D domain's boundary conditions are known, the global capacitance matrix with size $n \times n$ can be obtained through the solving of the Laplace equation. Only the nodes of conductors exist corresponding to the global capacitance matrix. If some of the boundary conditions are unknown, the global capacitance matrix cannot be obtained. One matrix, i.e., the BCM, is presented. For the BCM, the nodes of both conductors and dielectrics exist. While using the BEM to solve the Laplace equation, the BCM describes the relationship between the potential and the flux of one node in the 3-D field.

Some requests to boundary elements corresponding to the BCM should be satisfied so as to fasten the whole computation, such as: 1) the elements of the same conductors should be condensed as only one node and 2) the elements with the boundary condition IBC should be eliminated.

The computation of the BCM will be presented in Section III-B according to these requests.

B. Computation of the BCM

When computing the BCM, there are two kinds of 3-D domains in capacitance extraction: a domain with single dielectric and a domain with multiple dielectrics.

1) *BCM of the 3-D Domain With Single Dielectric:* As described previously, the Laplace equation is solved to compute the capacitance. Using the BEM, the Laplace equation (1) can be transferred into the direct boundary integration equation (DBIE) [3] in the 3-D domain Ω as follows:

$$c_s u_s + \int_{\partial\Omega_k} q^* u d\Gamma = \int_{\partial\Omega_k} u^* q d\Gamma, \quad k = 1, 2, \dots, M \quad (7)$$

where $u^*(s, t) = (1)/(4\pi r(s, t))$ is the fundamental solution of the Laplace equation, and $q^* = \partial u^*/\partial \mathbf{n}$. \mathbf{n} is the outward normal direction on the boundary. $\partial\Omega_k$ is the boundary of the k th dielectric domain Ω_k . u_s is the potential at the source point. c_s is a coefficient determined by the geometry at the source point. u and q are the potential and flux, respectively, of one point on the boundaries surrounding the 3-D domain Ω_k . Equation (7) should be satisfied at any point on the boundaries.

The boundary $\partial\Omega_k$ ($k = 1, \dots, M$) can be divided into many boundary elements. If the shape function within each boundary element is constant, (7) can be written by

$$0.5u_i^k + \sum_{j=1}^{N_k} u_j^k \int_{\Gamma_j^k} q^* d\Gamma = \sum_{j=1}^{N_k} q_j^k \int_{\Gamma_j^k} u^* d\Gamma, \quad i = 1, \dots, N_k; \quad k = 1, \dots, M \quad (8)$$

where N_k is the number of boundary elements on the boundary $\partial\Omega_k$. Γ_j^k is the j th boundary element on $\partial\Omega_k$. u_j^k and q_j^k is the potential and flux on Γ_j^k . All the integration based on the constant shape function can be computed by an analytical or semianalytical formula [25].

Equation (8) can be written in the matrix form as follows:

$$H\mathbf{u} = G\mathbf{q} \quad (9)$$

where H and G are the coefficient matrices. \mathbf{u} and \mathbf{q} are the column vectors of potential and flux, respectively, of all the boundary elements.

Usually the matrix G is nonsingular. Equation (9) can then be turned into

$$C\mathbf{u} = \mathbf{q}, \quad \text{where } C = G^{-1}H. \quad (10)$$

The vectors \mathbf{u} and \mathbf{q} contain all the variables of the elements on the boundary of dielectrics and conductors.

According to the first request mentioned in A of the elements, all these elements belonging to the same conductor should be condensed into only one element with the superposition of the

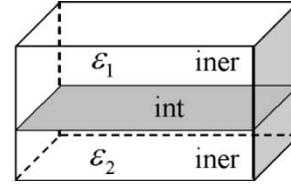


Fig. 1. 3-D domain with two dielectrics.

variables q on these elements. This superposition will not decrease accuracy.

It is supposed that there are a total of N elements, where 1 to m are on the boundary of dielectrics and $m + 1$ to N are on the boundaries of conductors. We assume that these elements belong to l conductors. The matrix C with size $N \times N$ can be transferred into matrix C' with size $(m + l) \times (m + l)$, which is satisfied by the following:

$$c'_{ij} = \begin{cases} c_{ij}, & i \leq m; \quad j \leq m \\ \sum_{(\Gamma_k \in \text{conductor } i)} \left(\int_{\Gamma_k} d\Gamma \right) c_{kj}, & i \leq m; \quad j > m \\ \sum_{(\Gamma_k \in \text{conductor } j)} c_{ik}, & i > m; \quad j \leq m \\ \sum_{(\Gamma_k \in \text{conductor } i)} \left(\int_{\Gamma_k} d\Gamma \right) \sum_{(\Gamma_r \in \text{conductor } j)} c_{kr}, & i > m; \quad j > m. \end{cases} \quad (11)$$

After the condensing, a smaller matrix is obtained. Such a matrix C' is exactly the BCM of the domain Ω with a single dielectric.

2) *BCM of the 3-D Domain With Multiple Dielectrics:* In the 3-D domain with multiple dielectrics, the second request mentioned in A should be satisfied. Those elements in the interface of dielectrics should be eliminated.

First, let us consider one simple example with only two dielectrics, as shown in Fig. 1. Using the BEM, (8) is satisfied in both domains with dielectrics 1 and 2 separately. In dielectric 1, the following formula can be obtained based on the BEM:

$$\begin{bmatrix} C1_{\text{iner,iner}} & C1_{\text{iner,int}} \\ C1_{\text{int,iner}} & C1_{\text{int,int}} \end{bmatrix} \begin{bmatrix} \mathbf{u1}_{\text{iner}} \\ \mathbf{u1}_{\text{int}} \end{bmatrix} = \begin{bmatrix} \mathbf{q1}_{\text{iner}} \\ \mathbf{q1}_{\text{int}} \end{bmatrix} \quad (12)$$

where the subscript int denotes the elements in the interface, and the subscript iner denotes all the other elements. The BCM of dielectric 1 ($C1$) can be obtained as (10). It can be divided into four sub-matrices as $C1_{\text{iner,iner}}$, $C1_{\text{iner,int}}$, $C1_{\text{int,iner}}$, and $C1_{\text{int,int}}$. These sub-matrices are related to the corresponding elements.

Similarly, in dielectric 2, the BCM $C2$ can be divided into four sub-matrices, which are satisfied with the following formula:

$$\begin{bmatrix} C2_{\text{iner,iner}} & C2_{\text{iner,int}} \\ C2_{\text{int,iner}} & C2_{\text{int,int}} \end{bmatrix} \begin{bmatrix} \mathbf{u2}_{\text{iner}} \\ \mathbf{u2}_{\text{int}} \end{bmatrix} = \begin{bmatrix} \mathbf{q2}_{\text{iner}} \\ \mathbf{q2}_{\text{int}} \end{bmatrix}. \quad (13)$$

On the interface of two dielectrics, the boundary condition IBC should be satisfied. The variables on the interface should be satisfied as

$$\begin{cases} \mathbf{u1}_{\text{int}} = \mathbf{u2}_{\text{int}} \\ \varepsilon_1 \mathbf{q1}_{\text{int}} + \varepsilon_2 \mathbf{q2}_{\text{int}} = 0. \end{cases} \quad (14)$$

According to (12)–(14), vectors $\mathbf{u1}_{\text{int}}$, $\mathbf{u2}_{\text{int}}$, $\mathbf{q1}_{\text{int}}$, and $\mathbf{q2}_{\text{int}}$ can be eliminated. Thus, we can obtain

$$C_b \mathbf{u} = \mathbf{q} \quad (15)$$

where

$$C_b = Z1 - Z2 \cdot Z3^{-1} \cdot Z4 \quad (16)$$

$$Z1 = \begin{bmatrix} C1_{\text{iner,iner}} & 0 \\ 0 & C2_{\text{iner,iner}} \end{bmatrix}$$

$$Z2 = \begin{bmatrix} C1_{\text{iner,int}} \\ C2_{\text{iner,int}} \end{bmatrix} \quad (17)$$

$$Z3 = [\varepsilon_1 C1_{\text{int,int}} + \varepsilon_2 C2_{\text{int,int}}]$$

$$Z4 = [\varepsilon_1 C1_{\text{int,iner}}, \varepsilon_2 C2_{\text{int,iner}}]$$

and

$$\mathbf{u} = \begin{bmatrix} \mathbf{u1}_{\text{iner}} \\ \mathbf{u2}_{\text{iner}} \end{bmatrix} \quad \mathbf{q} = \begin{bmatrix} \mathbf{q1}_{\text{iner}} \\ \mathbf{q2}_{\text{iner}} \end{bmatrix}.$$

Equation (16) is the BCM of the 3-D field with two dielectrics.

In the domain with multiple dielectrics, the BCM can be obtained similarly as in the domain with two dielectrics.

C. Get a Global Capacitance Matrix From the BCM

According to the requests of the BCM, the global capacitance matrix can be easily computed by applying the boundary condition NBC. The BCM C_b can then be divided into four sub-matrices as C_{b1} , C_{b2} , C_{b3} , and C_{b4} , which are satisfied with the following:

$$\begin{bmatrix} C_{b1} & C_{b2} \\ C_{b3} & C_{b4} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{\text{cond}} \\ \mathbf{u}_{\text{diel}} \end{bmatrix} = \begin{bmatrix} \mathbf{q}_{\text{cond}} \\ \mathbf{q}_{\text{diel}} \end{bmatrix} \quad (18)$$

where the subscript cond denotes the elements of conductors, and the subscript diel denotes those of dielectrics. Since all the elements with the IBC have been eliminated, the elements with subscript diel satisfy the NBC. According to (3), (18) can be turned into

$$(C_{b1} - C_{b2} C_{b4}^{-1} C_{b3}) \mathbf{u}_{\text{cond}} = \mathbf{q}_{\text{cond}}. \quad (19)$$

Let $C_r = C_{b1} - C_{b2} C_{b4}^{-1} C_{b3}$, which is the required global capacitance matrix.

Section IV will present our hierarchical approach to compute the global capacitance matrix based on the BCM called the HBBEM.

IV. HBBEM FOR 3-D CAPACITANCE COMPUTATION

Hierarchical computation usually divides one large problem into many small pieces in order to accelerate the computation. In 3-D capacitance extraction, our hierarchical computation will divide the 3-D domain into several sub-regions, which are called BEM blocks. The local computation is the solution of the BCM in each BEM block. All the known conditions are used while solving the BCM. The BCM in each block stands for the local network in each BEM block. Only a few unknown variables are left in the local computation, and after merging all the BCM of

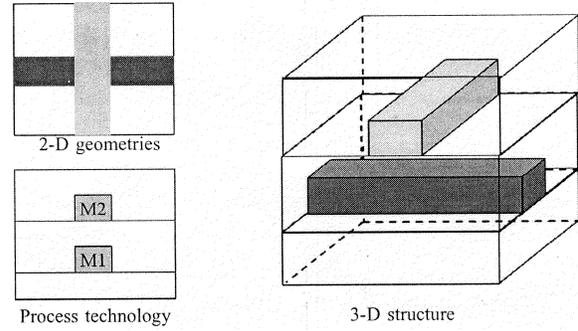


Fig. 2. Generation of the 3-D structure by combination of 2-D geometries and process technology in a real layout.

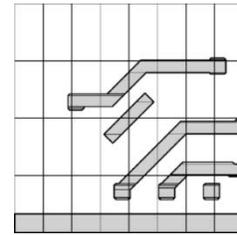


Fig. 3. Partition of the 2-D interconnect geometry in one layer.

the BEM blocks, the global reduced network can be obtained, which is the required global capacitance matrix.

Based on the BCM, one rapid approach is presented to compute the global capacitance matrix of the whole 3-D domain using the 3-D BEM blocks. It has the following four steps.

- Step 1) Hierarchical partition of the 3-D domain so as to generate the BEM blocks.
- Step 2) Computation of the BCM in each BEM block.
- Step 3) Applying the known conditions to all the BCMs.
- Step 4) Hierarchical combination of the BCM in all the BEM blocks to get the global capacitance matrix.

A. Hierarchical Partition of the 3-D Domain

Currently, the 3-D interconnect structure is usually generated by 2-D geometries from the layout and design process technology [24]. 2-D geometries include the information of interconnect, such as the shape, layer number, etc. The process technology is used to describe the cross-sectional structure, such as the thickness of interconnect, thickness of the dielectric, etc. The 3-D interconnect structure can be generated with the geometry and process technology, as shown in Fig. 2. The NBC conditions should be satisfied on the outer surface of the 3-D domain.

According to the generation of the 3-D structure, the partition of the 3-D structure can also be generated from the following two aspects: partition of the 2-D geometries and partition of the process technology.

1) *Hierarchical Partition of the 2-D Geometries*: The geometries of the interconnect can be obtained from the layout. All the polygons of the interconnect will be in some layers. Therefore, all these polygons can be assigned to some layers. For each layer, all the polygons of the interconnect can be divided into $m_x \times m_y$ blocks, as shown in Fig. 3. The numbers of m_x and m_y are determined by the size of each BEM block. In our approach, the size of each BEM block is determined by the

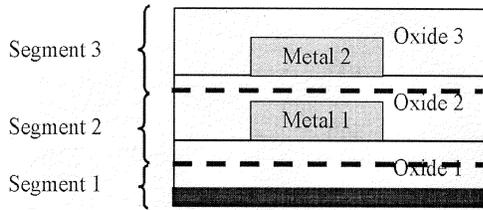


Fig. 4. Partition of the process technology.

minimum feature size λ of the interconnect. Here, the length l and width w of the BEM block are set as follows:

$$l = w = 4 * \lambda. \quad (20)$$

m_x and m_y can then be obtained as follows:

$$m_x = \lfloor L_{win}/l \rfloor \quad m_y = \lfloor W_{win}/w \rfloor. \quad (21)$$

where L_{win} and W_{win} are the length and width of the window to be extracted in the layout.

2) *Partition of the Process Technology*: The process technology defines the structure in the Z -direction. Therefore, the 3-D domain can be divided into several parts in the Z -direction if the process technology can be partitioned into several process segments. Currently, almost all the interconnect structures are the layer structure. It is easy to make such a partition of the process.

The simplest way is to place the partitions exactly on the interface of layers, but such a partition is not a good one. Usually the interconnects exactly touch the interface so that the geometries of interface are very complex. It is difficult for implementation. Additionally, the complexity of the interface will make more boundary elements in the interface, which may increase the computation time in the merging process. In order to optimize the computation, the partition of the process technology will abide by the following rules.

- The number of process segments in the Z -direction is the same as the number of layers.
- The partition position of the segments in the Z -direction is at the middle surface of the top of metal and the bottom of the upper dielectric.

The partition can be seen in Fig. 4. The process with three oxides can be partitioned into three process segments.

3) *Organization of the Partition*: For each layer, the geometries of the interconnect are clipped by $m_x \times m_y$ blocks. Since each layer has a corresponding process segment, each block has one 3-D structure according to its corresponding process segment and geometries. Such a 3-D structure forms one 3-D BEM block.

In order to get a convenient and effective partition, the hierarchical binary tree is invoked to make the organization shown in Fig. 5.

If we use the full binary tree, the original domain should be divided into 2^n parts, where n is the depth of the tree. Each leaf of the tree stands for one block of the original domain. Each leaf can build one 3-D BEM block with the process technology. This procedure can be easily implemented using the post-order traversal of the tree.

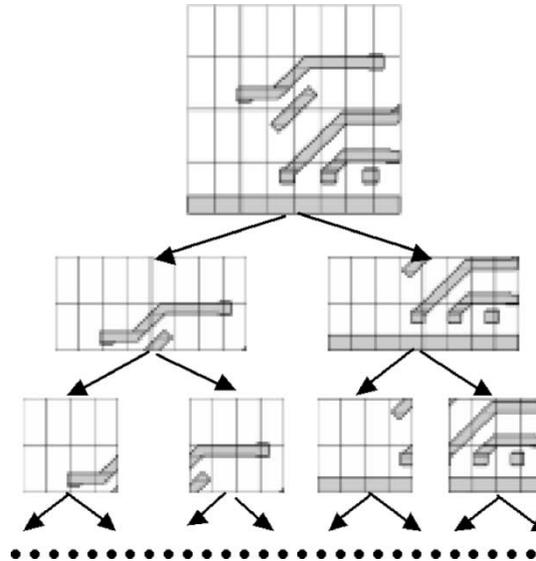


Fig. 5. Hierarchical organization of the partition.

B. Computation of the BCM in all BEM Blocks and Reuse Technology

In the previous sections, the computation of the BCM of 3-D domains has been presented. Thus, the BCM of all the leaves of the hierarchical tree can be obtained using the post-order traversal of the tree.

Due to the hierarchical approach, the reuse technology can be used in the computation of the BCM. Currently, in the HBBEM, we can reuse the BCM result if the 3-D domain contains no conductors. That can improve the speed.

C. Applying the Known Condition

In order to reduce the number of unknown variables, the known condition should be applied in each BEM block.

As described in Section II, there are two kinds of boundary condition in capacitance extraction: the DBC, as shown in (2), and the NBC, as shown in (3). Since we do not preset the bias on the conductors, the DBC will not be applied. The NBC should be applied on the outer surface of the whole 3-D domain. Therefore, on some surfaces of the BEM block, the NBC is the known condition.

While computing the BCM of one BEM block, the NBC should be applied to reduce the number of unknown variables.

For example, the BCM C_b is satisfied with the following:

$$\begin{bmatrix} C_{b_{other,other}} & C_{b_{other,nbc}} \\ C_{b_{nbc,other}} & C_{b_{nbc,nbc}} \end{bmatrix} \begin{bmatrix} \mathbf{u}_{other} \\ \mathbf{u}_{nbc} \end{bmatrix} = \begin{bmatrix} \mathbf{q}_{other} \\ \mathbf{q}_{nbc} \end{bmatrix} \quad (22)$$

where subscript nbc denotes the elements with the NBC boundary condition, and the subscript other denoted other elements. Matrix C_b can be divided into four sub-matrices $C_{b_{other,other}}$, $C_{b_{other,nbc}}$, $C_{b_{nbc,other}}$, and $C_{b_{nbc,nbc}}$ according to the number of elements with the NBC boundary condition.

Since $q_{nbc} = 0$, the following formula can be obtained from (22):

$$C'_b \mathbf{u}_{other} = \mathbf{q}_{other} \quad (23)$$

where

$$C'_b = C_{\text{bother,other}} - C_{\text{bother,nbc}} C_{\text{nbc,nbc}}^{-1} C_{\text{nbc,other}}. \quad (24)$$

C'_b is the BCM after applying the boundary-condition NBC. The size of C'_b is much smaller than that of C_b .

Next, how to combine the BCM of two adjacent 3-D BEM blocks will be presented.

D. Hierarchical Combination of 3-D BEM Blocks

According to the hierarchical organization, the BCM of each node of the binary tree can be obtained by merging the BCM of its two child nodes. The combination of BCMs in two 3-D BEM blocks is very similar to the BCM computation of the domain with two dielectrics, which was presented in Section III-B.2. Only the continuous condition is different from (14) according to our partition assumption. The following continuous conditions should be satisfied in the interface with the IBC:

$$\begin{cases} \mathbf{u}1_{\text{inter}} = \mathbf{u}2_{\text{inter}} \\ \mathbf{q}1_{\text{inter}} + \mathbf{q}2_{\text{inter}} = 0. \end{cases} \quad (25)$$

Therefore, the result of the matrix is also different from (17) as follows:

$$Z3 = [C1_{\text{int,int}} + C2_{\text{int,int}}]. \quad (26)$$

Hence, the formula of the combination BCM of C_{b1} and C_{b2} can be computed.

In the binary tree of the BEM blocks, the BCM of each node can be obtained by combining the BCMs of its two child nodes. When the BCM of the tree's root is obtained, the combination is finished. Since all of the known conditions of the NBC have been applied, the BCM of the root is the required global capacitance matrix.

E. Flow of the HBBEM Approach

The global flow of the hierarchical approach can be described as shown in Fig. 6.

In the beginning of the approach, two kinds of input data should be included: the polygon information of all the layers and the process information of all the layers. The hierarchical partition of the 3-D domain can then be completed separately by the partition of the polygons and process technology. All the 3-D BEM blocks will be formed after the partition. After the computation of the BCM in all the BEM blocks, the boundary-condition NBC is applied. According to the continuous boundary condition between two adjacent BEM blocks, the BCM can be combined. Finally, the capacitance matrix can be easily formed after merging all the BCMs of the BEM blocks.

F. Discussion About Gridding

In any kind of numerical method, the gridding is important for both accuracy and speed. In the HBBEM, the gridding can be determined by a tradeoff in accuracy and speed, especially in the interface region between the two BEM blocks.

According to the capacitance computation, it is better that the gridding is dependent on the feature size λ of the interconnect. Therefore, in the HBBEM, the size of each boundary element is

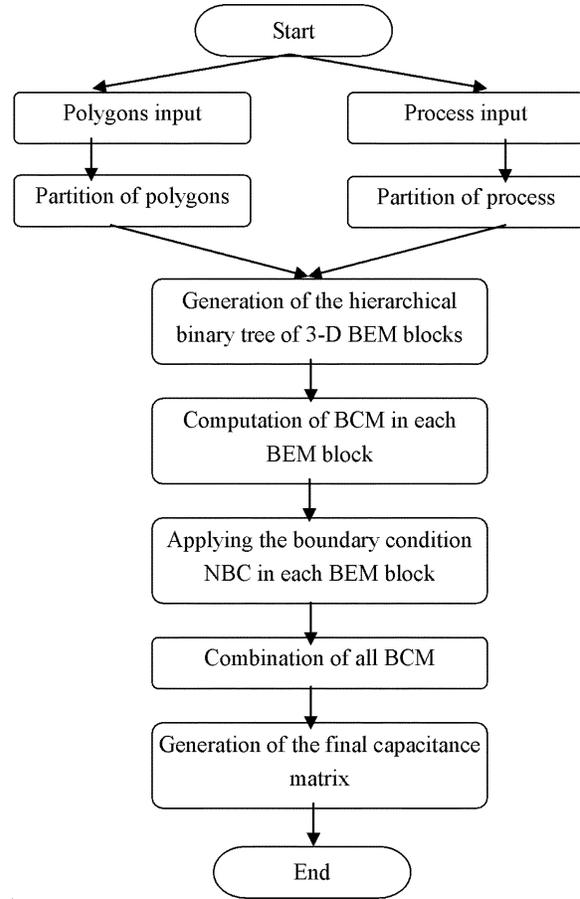


Fig. 6. Flow of the program.

dependent on λ . In the 3-D computation, the size of the element can be described by d_x, d_y , and d_z , which separately determine the size along three directions. In the HBBEM, one parameter α is used as follows:

$$d_x = d_y = d_z = \alpha\lambda. \quad (27)$$

In order to get the optimal parameter of α , a series of tests have been done with the different feature sizes of the interconnect from 0.5 to 0.07 μm . The 3-D structure data, such as the minimum pitch and aspect ratio of interconnects, are referred to in [27]. Fig. 7 shows the effect of α on both accuracy and speed when the feature size λ is 0.15. From the curve, we can get the range of parameter α with good performance on both accuracy and speed ($0.5 < \alpha < 1.0$).

The tests for all the feature sizes show that the range of α for good performance is between 0.5–0.8. Therefore, in order to get a good tradeoff of accuracy and speed, let $\alpha = 0.65$ in the HBBEM. The numerical results listed in Section IV-G show the good performance with such a parameter.

G. Time Complexity Discussion

According to the flow of the approach, the computational time is mainly dependent on two parts: the computation of the BCM and the combination of the BCM.

Since the size of each 3-D BEM block in the leaf node can be considered as constant, the local computational time in each

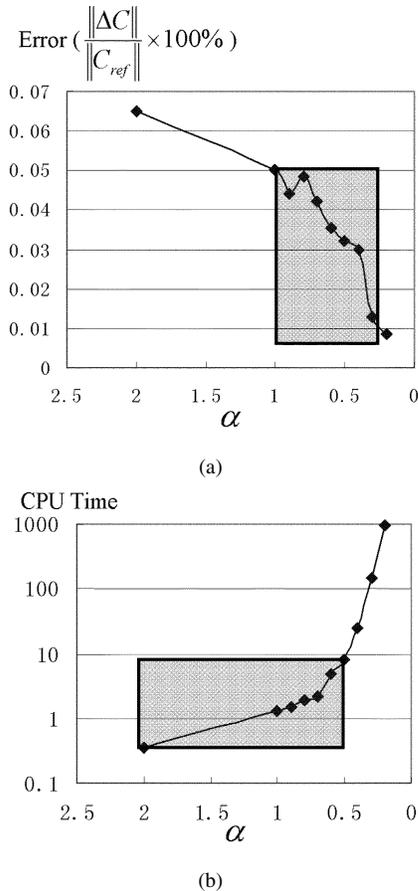


Fig. 7. α and performance of the HBBEM with the feature size $\lambda = 0.15$. (a) Effect on accuracy. (b) Effect on speed.

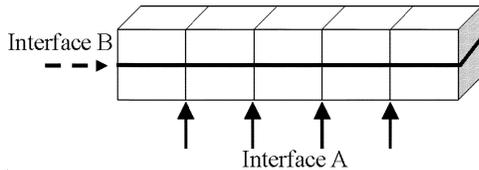


Fig. 8. Two types of interface.

3-D BEM block can be as constant. Therefore, the time of computation of the BCM depends on the number of the 3-D BEM blocks.

The combination of the BCM depends on the interface gridding and the interface number. The interface gridding can be considered as constant. The interface number is dependent on the organization of the hierarchical trees of the 3-D domain. If the 3-D domain is a long tunnel shape, as shown in Fig. 8, there will be two types of the organization, i.e., A and B.

If type A is used, the gridding of the interface is constant. The number of the interface is linear growth with the length of the domain. Thus, the total computation time is linear growth with the size of the 3-D domain in the other direction. Such a result can be shown in the numerical results of the cross bus structure, which are listed in Section V. However, if type B is used, the number of interfaces is grown linearly. The gridding of the interface is grown linearly with the dimension. The total computation time will not grown linearly with the size of the 3-D domain. Therefore, the organization in the HBBEM will generate the interface with type A.

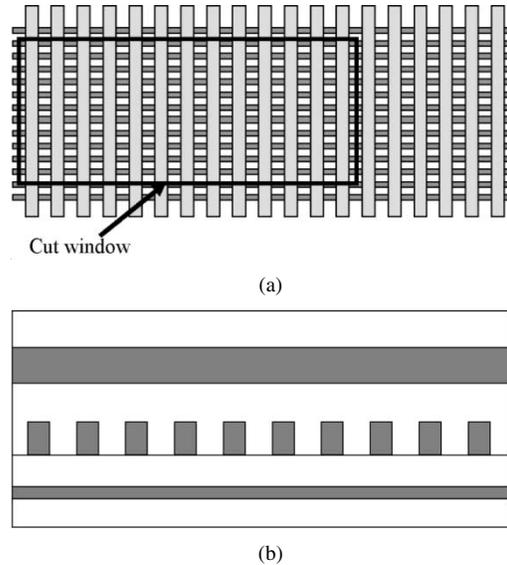


Fig. 9. Cross-bus structure. (a) Top view and cut window. (b) Cross-sectional structure.

In most case, the 3-D domain for capacitance extraction is usually the long tunnel shape. However, if the 3-D domain is not a long tunnel shape, the computational time will not be linear with the size of domain. Even so, the HBBEM is still very fast if the 3-D domain is not very large.

V. NUMERICAL RESULTS

Here, the HBBEM method is used to analyze the cross-bus structure first in order to show the hierarchical efficiency in time complexity. One simple 3-D structure is then tested, whose results are compared with those in [18] and [25]. Finally, a complex 3-D case cut from the real layout is used to depict the performance of the HBBEM method, whose computational result is compared with the 3-D field solver software "RAPHAEL." The NBC conditions are used on the outer surface of all the 3-D structures.

A. Cross-Bus Structure

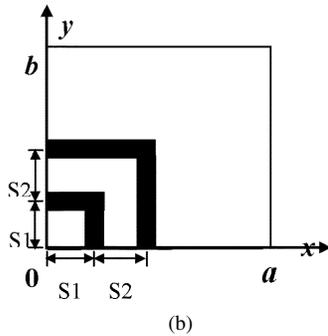
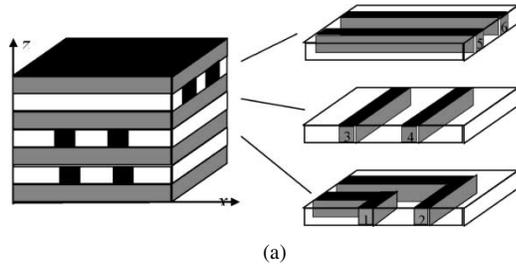
The structure is shown in Fig. 9. There are three metal layers totally above the substrate. In METAL 1, the cross-sectional size of every line is 1×0.25 , the gap between each two conductor is one. In METAL 2, the cross-sectional size of each line is 0.5×0.75 , the gap between two conductors is also 0.5. In METAL 3, the cross-sectional size of each line is 1×0.75 , the gap between two conductors is one. All the lines are orthogonal in different layers. Counted from the bottom, the thickness of every dielectric layer is 0.335, 0.75, 1.60, and 1.60. All length parameters above are in micrometers. The relative permittivity of every layer is 3.9. They are shown in Fig. 9(b).

The window sizes of the 3-D domain tested are 10×10 , 20×10 , 30×10 , and 40×10 .

The computer result is listed in Table I. C_c stands for the self-capacitance of the line on Metal 2, which is in the middle of the cut window. C_r and C_l is the coupling capacitance between that line and the one located at its right and left sides, separately. C_u and C_d is the coupling capacitance between that line and any line in Metals 3 and 1.

TABLE I
 TIME AND ACCURACY OF THE HBBEM FOR A CROSS-BUS STRUCTURE

| Window Size | 10x10 | | 20x10 | | 30x10 | | 40x10 | |
|------------------|---------|-------|---------|-------|---------|-------|---------|-------|
| | Raphael | HBBEM | Raphael | HBBEM | Raphael | HBBEM | Raphael | HBBEM |
| Conductor number | 21 | | 31 | | 41 | | 51 | |
| Time(s) | 2061 | 14 | 2933 | 30 | 4954 | 45 | 6334 | 64 |
| C_c (fF) | 2.27 | 2.25 | 4.568 | 4.516 | 6.882 | 6.776 | 9.237 | 9.037 |
| C_r (fF) | 0.67 | 0.652 | 1.343 | 1.38 | 2.019 | 2.06 | 2.682 | 2.75 |
| C_l (fF) | 0.669 | 0.65 | 1.341 | 1.37 | 2.013 | 2.05 | 2.673 | 2.74 |
| C_u (fF) | 0.103 | 0.97 | 0.104 | 0.97 | 0.105 | 0.97 | 0.105 | 0.97 |
| C_d (fF) | 0.073 | 0.079 | 0.073 | 0.079 | 0.073 | 0.079 | 0.073 | 0.079 |


 Fig. 10. One simple 3-D structure. (a) 3-D view. (b) Top view of the layer with bends $a = b = 13$, $S1 = 3.5$, and $S2 = 3$.

From Table I, we can see that the computer time is almost grown linearly with the size of the cut window. That is the efficiency of the hierarchical algorithm. All the self-capacitance and coupling capacitance are as accurate as Raphael.

B. One Simple 3-D Structure

The structure is shown in Fig. 10(a). The size of every straight line is $1 \times 1 \times 13$, the gap between conductors 3 and 4, as well as conductors 5 and 6, is three. The distance between the straight line and the border is four. The size of the cross section of every bend is 1×1 ; other geometric parameters of the bends are shown in Fig. 10(b). Counted from the bottom, the thickness of every dielectric layer is one, one, two, one, one, one, and one. All length parameters above are in millimeters. The relative permittivity of every layer is two, three, three, four, four, five, and five.

We have calculated the capacitance matrix by the HBBEM; corresponding results using SpiceLink and the overlapped domain-decomposition method (ODDM) are provided by [18] and the QMM by [25]. Only C_{11} , C_{22} , C_{44} , and C_{66} are listed in Table II. The discrepancy among the results obtained with the three methods is within 2%. In the HBBEM method, 8×8 partition is applied. Using a Sun Ultra-Sparc 20, the CPU time and memory size used by these methods are shown in Table II. The HBBEM is approximately 300 times faster than SpiceLink, ap-

 TABLE II
 CAPACITANCE, TIME, AND MEMORY FROM THE SPICELINK, ODDM, AND HBBEM

| | C_{11} (fF) | C_{22} (fF) | C_{44} (fF) | C_{66} (fF) | Time(s) | Mem(MB) |
|-----------|---------------|---------------|---------------|---------------|---------|---------|
| SpiceLink | 0.669 | 1.29 | 1.54 | 2.53 | 1327 | 75.9 |
| ODDM | 0.680 | 1.29 | 1.52 | 2.54 | 122 | 2.7 |
| QMM | 0.682 | 1.31 | 1.54 | 2.53 | 58.4 | 3.80 |
| HBBEM | 0.673 | 1.33 | 1.58 | 2.52 | 3.7 | 2.52 |

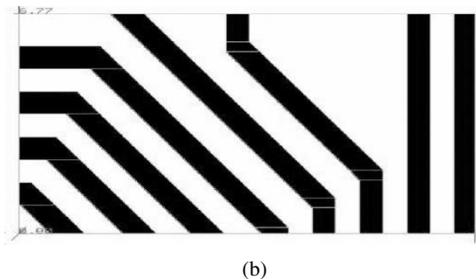
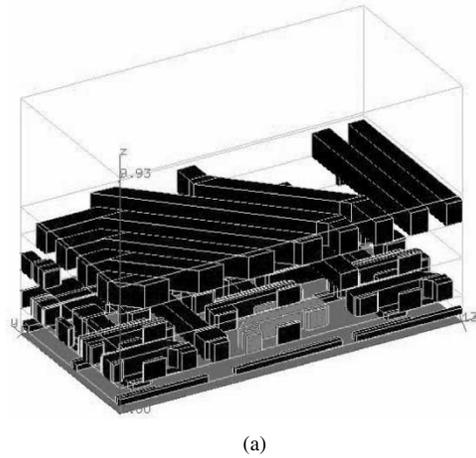


Fig. 11. Complex 3-D structure with bevels. (a) 3-D view. (b) Top view of layer "Metal4."

proximately 30 times faster than ODDM, and approximately 15 times faster than the QMM. Reuse technology can greatly take effect in this case to reduce the running time. The memory used by the HBBEM is similar to that used by ODDM, which is much smaller than that used by SpiceLink.

C. Complex 3-D Structure With Bevels

The 3-D structure is cut from the real layout. The 3-D view is shown in Fig. 11(a). The top view of the layer "Metal4" is shown in Fig. 11(b). Detailed information of the 3-D structure is listed in Table III. There are six stratified dielectrics in the 3-D domain with 264 conductors including the substrate. Some of conductors are bevel lines. All the conductors belong to 24 nets. Therefore, the global capacitance matrix is of size 24×24 .

TABLE III
DETAIL INFORMATION OF THE COMPLEX 3-D STRUCTURE

| Window Size | Dielectric Number | Conductor Number | Net Number |
|---|-------------------|------------------|------------|
| $13.5\mu\text{m} \times 6.7\mu\text{m}$ | 6 | 264 | 24 |

TABLE IV
CAPACITANCE, TIME, AND MEMORY FROM RAPHAEL AND THE HBBEM

| | Raphael | | | QMM | HBBEM |
|--------------|--------------|---------|---------|------|-------|
| | Default Grid | 5M Grid | 8M Grid | | |
| Time(s) | 86885 | 95103 | 178707 | 416 | 34 |
| $C_{66}(fF)$ | 922 | 897 | 872 | 862 | 881 |
| Error. (%) | 5.7 | 2.9 | ** | -1.1 | 1.0 |

We have calculated the capacitance matrix from net to net by the HBBEM and QMM [25], corresponding results using Raphael version 2000.2 [26] under different grids. Only self-capacitance of net 66 is listed in Table IV. Using a 248-MHz Sun Ultra E450, the CPU costs used by these methods are shown in Table IV. The HBBEM is approximately 3000 times faster than Raphael under a 5-M grid, which has comparable accuracy, and is approximately 12 times faster than the QMM. The capacitance reference value was calculated by Raphael under an 8-M grid, which is accurate enough.

The numerical results show that HBBEM is several thousands times faster than the field solver Raphael with comparable accuracy. Therefore, it is well suited for very large scale integration (VLSI) interconnect capacitance extraction with high speed and high accuracy. In fact, the CPU time listed in Table IV is the time to get only one column of the 24×24 global capacitance matrix for Raphael, but one global capacitance matrix can be gotten in approximately 34 s for the HBBEM.

VI. CONCLUSION

A hierarchical global field solver, i.e., the HBBEM, has been implemented, which uses 3-D BEM block technology and hierarchical computation in VLSI 3-D capacitance extraction. It is essentially different from local field solvers, such as the QMM in [25], etc. In the HBBEM, global computation is divided into many independent local computations that have a much smaller size. The 3-D partition is realized by combining the partition of the 2-D layout with that of process technology, which can reduce the complexity of the 3-D partition. The BCM is computed in each BEM block using all the known conditions. Reuse technology can save a lot of running time. Using the BCM combination can get the global matrix. In the QMM, the 3-D partition can accelerated the computation because of the sparse property of the direct BEM. However, all the partitioned mediums are interdependent. One linear system should still be formed to be solved in the QMM. The HBBEM gives out the required global capacitance matrix directly, while the QMM only gives out one column of the capacitance matrix.

The numerical results show that HBBEM costs much less in computational time compared with the local field solver in computing the global matrix. The HBBEM is much better than the local field solvers when computing the global capacitance matrix. Therefore, the HBBEM is very suitable for chip-level analysis, where the RC extraction should be high in accuracy and speed.

ACKNOWLEDGMENT

The authors would like to thank Prof. X. L. Hong, Electronic Design Automation (EDA) Group, Tsinghua University, Beijing, China, for his help and support. The helpful comments of the anonymous reviewers are also gratefully acknowledged.

REFERENCES

- [1] A. Premioli, "A new fast and accurate algorithm for the computation of microstrip capacitances," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, 14, pp. 642–648, Aug. 1975.
- [2] P. Benedek, "Capacitance of a planar multiconductor configuration on a substrate by a mixed order finite-element method," *IEEE Trans. Circuits Syst.*, vol. CAS-23, pp. 279–284, May 1976.
- [3] C. A. Brebbia, *The Boundary Element Method for Engineers*. London, U.K.: Pentech Press, 1978.
- [4] D. Korzec *et al.*, "Device and parasitic oriented circuit extractor," in *Proc. Int. Computer-Aided Design Conf.*, Rye, NY, 1987, pp. 430–433.
- [5] A. H. Zemanian, "A finite-difference procedure for the exterior problem inherent in capacitance computation for VLSI interconnects," *IEEE Trans. Electron Devices*, vol. 35, pp. 985–992, July 1988.
- [6] K. Nabors and J. White, "FastCap: A multipole-accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design*, vol. 10, pp. 1447–1459, Nov. 1991.
- [7] J. Chern *et al.*, "Multilevel metal capacitance models for CAD design synthesis systems," *IEEE Electron Device Lett.*, vol. 14, pp. 32–34, Jan. 1992.
- [8] M. Niewczak and A. Wojtasik, "Modeling of VLSI RC parasitics based on the network reduction algorithm," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 137–144, Feb. 1995.
- [9] M. Basel, "Accurate and efficient extraction of interconnect circuits for full-chip timing analysis," in *WESCON Conf. Rec.*, Nov. 7–9, 1995, pp. 118–123.
- [10] U. Choudhury and A. Sangiovanni, "Automatic generation of analytical models for interconnect capacitances," *IEEE Trans. Computer-Aided Design*, vol. 14, pp. 470–480, Apr. 1995.
- [11] O. E. Akcasu *et al.*, "'Net-an': A full three-dimensional parasitic interconnect distributed RLC extractor for large full chip applications," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 10–13, 1995, pp. 495–498.
- [12] K. L. Shephard and V. Narayanan, "Noise in deep submicron digital design," in *Proc. IEEE/ACM Int. Computer-Aided Design Conf.*, San Jose, CA, Nov. 1996, pp. 524–531.
- [13] N. D. Arora, K. V. Raol, R. Schumann, and L. M. Richardson, "Modeling and extraction of interconnect capacitances for multilayer VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. 15, pp. 58–67, Oct. 1996.
- [14] E. A. Dengi and R. A. Rohrer, "Hierarchical 2-D field solution for capacitance extraction for VLSI interconnect modeling," in *Proc. Design Automation Conf.*, June 9–13, 1997, pp. 127–132.
- [15] R. B. Iverson and Y. L. Le Coz, "Methodology for full-chip extraction of interconnect capacitance using Monte Carlo-based field solvers," in *Int. Simulation of Semiconductor Processes and Devices Conf.*, Sept. 8–10, 1997, pp. 117–120.
- [16] S. Y. Oh, K. Okasaki, J. Moll, O. S. Nakagawa, and N. Chang, "3D global interconnect parameter extractor for full-chip global critical path analysis," in *IEEE Electrical Performance of Electronic Packaging Topical Meeting*, Oct. 27–29, 1997, pp. 46–49.
- [17] W. Sun, W. W. M. Dai, and W. Hong, "Fast parameter extraction of general interconnects using geometry independent measured equation of invariance," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 827–836, May 1997.
- [18] Z. Zhu, H. Ji, and W. Hong, "An efficient algorithm for the parameter extraction of 3-D interconnect structures in the VLSI circuits: Domain decomposition method," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1179–1184, Aug. 1997.
- [19] E. A. Dengi and R. A. Rohrer, "Boundary element method macromodels for 2-D hierarchical capacitance extraction," in *Proc. Design Automation Conf.*, June 15–19, 1998, pp. 218–223.
- [20] E. A. Dengi, "A parasitic capacitance extraction method for VLSI interconnect modeling," Ph.D. dissertation, 1997.
- [21] W. Shi, J. Liu, N. Kakani, and T. Yu, "Fast hierarchical algorithm for 3-D capacitance extraction," in *Proc. Design Automation Conf.*, June 15–19, 1998, pp. 212–217.

- [22] W. Hong *et al.*, "A novel dimension-reduction technique for the capacitance extraction of 3-D VLSI interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 1037–1044, Aug. 1998.
- [23] Z. Zhu and H. Wei, "A generalized algorithm for the capacitance extraction of 3-D VLSI interconnects," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 2027–2030, Oct. 1999.
- [24] M. Bächtold *et al.*, "System for full-chip and critical net parasitic extraction for ULSI interconnects using a fast 3-D field solver," *IEEE Trans. Computer-Aided Design*, vol. 19, pp. 325–338, Mar. 2000.
- [25] W. Yu, Z. Wang, and J. Gu, "Fast capacitance extraction of actual 3-D VLSI interconnects using quasi-multiple medium accelerated BEM," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 109–119, Jan. 2003.
- [26] *Manual of Raphael 2000.2*, 2000.
- [27] *Overall Technology Roadmap Characteristics Table*, Semiconduct. Ind. Assoc., 2001.



Taotao Lu received the B.S. degree in mechanism engineering and M.S. degree in computer science from Tsinghua University, Beijing, China, in 1998 and 2001, respectively, and is currently working toward the Ph.D. degree in computer science and technology at Tsinghua University.

His main research interests are the parasitic interconnect parameter extraction in VLSI computer-aided design (CAD), especially in 3-D interconnect capacitance extraction. He is also involved with numerical computation methods on

the electromagnetic-field solution, especially on the BEMs.



Zeyi Wang received the Computational Mathematics degree from the Xian Jiaotong University, Xian, China, in 1965.

Since 1965, he has been with Tsinghua University, Beijing, China, where he is currently a Professor with the Department of Computer Science and Technology. From 1987 to 1988, he was a Visiting Scholar with Stanford University, where he was involved with 3-D device simulation on a parallel computer. His main research interests are the application and research of numerical methods,

including parallel computations in the areas of VLSI CAD such as circuit analysis, device simulation, and parasitic interconnect parameter extraction.



Wenjian Yu was born in Nanchang, China, in 1977. He received the B.S. and M.S. degrees in computer science from Tsinghua University, Beijing, China, in 1999 and 2001, respectively, and is currently working toward the Ph.D. degree in computer science and technology at Tsinghua University.

He has authored or coauthored approximately ten papers in international journals and conference proceedings. His main research interests are the application and research of numerical methods in VLSI CAD such as parasitic interconnect parameter extraction.