Fast Random Walk Based Capacitance Extraction for the 3-D IC Structures With Cylindrical Inter-Tier-Vias

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***Abstract*—3-D integrated circuits (3-D ICs) make use of the vertical dimension for smaller footprint, higher speed, lower power consumption, and better timing performance. In 3-D ICs, the inter-tier-via (ITV) is a critical enabling technique because it forms vertical signal and power paths. Accordingly, it is imperative to accurately and efficiently extract the electrostatic capacitances of ITVs using field solvers. Unfortunately, the cylindrical via shape presents major challenges to most of the existing methods. To address this issue, we develop a novel floating random walk (FRW) method by rotating the transition cube to suit the cylindrical surface, devising a special space management technique, and proposing accelerating techniques for structures with large-sized through-silicon-vias. Experiments on typical ITV structures suggest that the proposed techniques is up to hundreds times faster than a simple FRW approach and the boundary element method-based algorithms, without loss of accuracy. In addition, compared with extracting the square-approximation structures, the proposed techniques can reduce the error by 10×. Large and multidielectric structures have also been tested to demonstrate the versatility of the proposed techniques.**

***Index Terms*—3-D integrated circuit (3-D IC), capacitance extraction, floating random walk (FRW) method, monolithic inter-tier-via (MIV), through-silicon-via (TSV).**

I. Introduction

3-D INTEGRATED circuits (3-D ICs) are generally considered to be one of the most promising solutions that offer a path beyond the Moore's law. By integrating multiple tiers vertically, 3-D ICs provide smaller footprint, higher speed, lower power consumption, and better timing performance. They are in general two types of 3-D ICs: 1) die stacking and 2) monolithic integration. Die stacking-based 3-D ICs simply stack multiple 2-D dies fabricated through conventional process technologies using through-silicon-vias (TSVs) [1]–[4]. It is fully compatible with existing process technologies, but the TSVs are large in size to ensure proper wafer handling and alignment. On the other hand, monolithic integration uses monolithic inter-tier-vias (MIVs) to connect multiple device layers fabricated sequentially. It requires innovative fabrication process [5]–[8], but allows the MIV to be much smaller than the TSV. In this paper, we use inter-tier-via (ITV) to denote both TSV and MIV.

ITVs play a critical role in 3-D ICs to deliver signal and power vertically, and therefore their parasitics need to be accurately modeled. High-precision parasitic extraction for ITVs has become a key challenge due to the rising number of 3-D analog effects, narrowed performance margins, and time windows. Overestimation of ITV parasitics results in excessive guardbands, which impacts performance and degrades the benefits of the 3-D technology. On the other hand, underestimation of parasitics causes potential timing failures and yield loss.

Among the parasitics, the ITV coupling capacitance has attracted much attention, due to its large impact on timing and noise analysis. Most existing works focused on the ITVs electrical model and the extraction of its cylindrical metal-oxide-semiconductor (MOS) capacitance [1]–[3], [23]. Few works were devoted to the electrostatic coupling capacitances among ITVs and horizontal wires, especially in the context of general layout structures. In [4], a set of analytical formulas was proposed for the coupling capacitance among ITVs and wires. It was also revealed there, that the electrostatic capacitance can be comparable to the MOS capacitance, and should not be ignored. However, the technique was derived from the square-shape assumption of TSV, which obviously differs from the reality and may have large error. And, the analytical technique is only applicable to regular TSV placements, whereas its error for random TSV placement was shown to reach 20% [4]. More recently, Peng *et al.* [22] proposed a full-chip extraction method to model the TSV-to-wire coupling. The method is based on the idea of pattern matching, and needs excessive computation for building up the capacitance library for a given process technology.

A more accurate approach to extract the parasitic capacitance of ITVs is to use electrostatic field solvers [9]–[18], [20], [24], [25], [27]. Field solvers for capacitance extraction are mainly attributed to two categories: 1) the boundary element method (BEM) [15]–[18], [24] and 2) floating random walk (FRW) method [10]–[12], [14], [20], [25]. Generally speaking, BEM runs faster than the FRW method for small- and medium-size problems. Yet its accuracy largely depends on the quality of boundary discretization and is therefore not very stable. On the other hand, the FRW method is a discretization-free method, and thus enjoys the advantages of

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better scalability for large structures, tunable accuracy, higher parallelism, etc. Unfortunately, there is no existing work in literature where these methods are applied to the ITV capacitance extraction. The relevant difficulty may be caused by the cylindrical shape of ITV.

If one employs BEM, a polyhedron should be used to well approximate the cylinder shape. This may cause a dense panel discretization. Taking into account the large dimensions of TSV, we can anticipate that such approximation can induce a large number of unknowns and large computational cost. On the other hand, the existing FRW algorithms for capacitance extraction assume that the considered geometries are all rectilinear-shaped [10]–[12], [14], [20], [25]. This limits their application only to the Manhattan geometries of interconnect wires in digital circuits. One naive solution is to approximate the cylindrical ITV with square-shape objects, but as we will demonstrate through experiments, the approximation causes large error. An FRW method using spherical transition domains, also known as the walk on sphere method, was recently proposed to handle 2-D non-Manhattan geometries [29], whose core idea is to facilitate the construction of transition spheres with a distance map. However, generating the distance map with sufficient resolution needs considerable computational cost. Therefore, the method is not feasible for actual 3-D large-scale structures, or not as practical as the space management techniques [12].

In this paper, we propose a novel method for the parasitic capacitance extraction considering the cylindrical-shape ITVs. We first reveal the errors brought by the square approximation of cylinder with several typical ITV structures. Then, based on the FRW algorithm, an approach with rotated transition cubes is proposed to accurately model the cylindrical ITVs. A special space management technique is also devised to efficiently handle general large-scale structures in 3-D ICs. Considering the largely different dimensions of TSV and conventional interconnect wire in the simulated structure, techniques are proposed to accelerate the convergence rate of the FRW procedure. Numerical experiments validate the accuracy of the proposed techniques, which show that we can reduce the error caused by the square-approximation approach by more than $10\times$ with negligible or small runtime overhead. Compared with the fast BEM solvers [15], [16], the proposed FRW-based method exhibits several tens to hundred times speedup and huge memory save, while guaranteeing stable accuracy. In addition, experiments have been carried out to show the scalability of the proposed method to large structures and its feasibility to actual multidielectric structures.

The main contributions of this paper are as follows.

1) It is the first work that directly extracts the capacitances of cylindrical ITVs without geometric approximation, and also the first work to handle non-Manhattan geometries with the random walk method using the cubic transition domains. We rotate the transition domain to make it touching the cylindrical surface of an ITV.
2) A special space management techniques is proposed to handle structures including a large number of ITVs, in order to keep the advantages of the FRW algorithm for large-scale structures. For structures with several hundred ITVs, this technique brings $8\times$ speedup.
3) A strategy for the placement of Gaussian surface and an optimized importance sampling scheme are proposed for the structure including large TSVs. With these special treatment, the FRW-based capacitance extraction is accelerated by over $10\times$ without loss of accuracy.

The rest of this paper is organized as follows. The background of modeling ITVs and the FRW algorithm for capacitance extraction are briefly introduced in Section II. We also demonstrate the errors caused by approximating the cylindrical ITVs with square-shape objects in Section II. The FRW-based capacitance extraction techniques which accurately consider the ITVs cylindrical shape are proposed in Section III. They include the FRW approaches employing Manhattan and rotated transition cubes, and an efficient space management technique. In Section IV, specific techniques to accelerate the extraction of structures with TSVs are proposed. We discuss how to apply the proposed method to the sign-off verification in Section V. The numerical results are given in Section VI, which validate the efficiency of the proposed techniques and compare the proposed method with two fast BEM-based solvers. Finally, we draw the conclusion. Some preliminary results of this paper were presented in [21]. We extend it with the third contribution, more numerical results and more technical details.

II. Background

A. Modeling of ITV Capacitances in 3-D ICs

There are in general two types of 3-D ICs: 1) die stacking with TSVs and 2) monolithic integration with MIVs. The TSVs can be fabricated with three technologies: 1) TSV-first; 2) TSV-middle; and 3) TSV-last. Under the TSV-first technology, devices and TSVs are fabricated first, and then metal layers are deposited. So, a TSV is surrounded by other TSVs laterally, and by wires mostly vertically [see Fig. 1(a)]. With the TSV-last technology, TSVs are fabricated after metal deposition, which makes them go through all the layers from the substrate to the topmost metal layer. Therefore, a TSV is surrounded by other TSVs laterally and by interconnect wires laterally and vertically [see Fig. 1(b)]. TSV is of cylinder shape, and much larger than conventional via (with typically 5 μm diameter, and height/diameter $= 10$).

In Fig. 1, we show the capacitive couplings among TSVs and wires. C_{TT} and C_{TD} are the capacitances between two TSVs, and between TSV and device, respectively. They involve the semiconductor effects in silicon substrate. In previous works (see [1]–[4]), the circuit model to capture the coupling among TSVs has been proposed. For example, Fig. 2 shows an equivalent circuit model for the coupling between two TSVs. C_{MOS} stands for the MOS capacitance with the substrate acting as the bulk and the TSV metal acting as a gate. C_{MOS} includes two factors, i.e., the cylindrical oxide capacitance due to TSV liner, and the depletion capacitance [3]. They can be calculated with the formulas given in [3]. C_{si} and R_{si} in Fig. 2 are the capacitance and resistance of silicon, with its dielectric and conductor properties both taken into account. Note that the capacitances in Figs. 1 and 2 are mostly electrostatic capacitance, except the semiconductor capacitance C_{MOS}.

Most of existing works, except [4], [22], paid attention to the calculation of the MOS capacitance component in C_{TT} and C_{TD}, rather than the electrostatic capacitance component and C_{TW} shown in Fig. 1. In [4], an analytical approach was

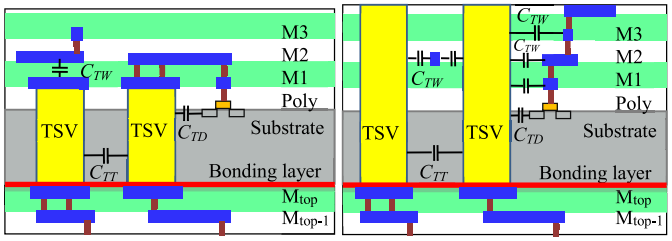

Fig. 1. (a) Cross-sectional views of the TSV-first technology. (b) TSV-last technology for the parallel 3-D IC.

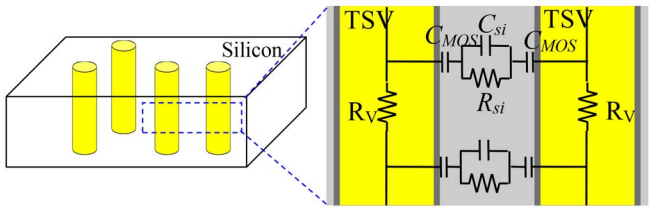

Fig. 2. Cylindrical TSVs in silicon, with relevant circuit model.

proposed to approximately calculate the electrostatic capacitances of TSVs, whose results showed that the electrostatic capacitance (~32.2 fF excluding TSV-to-wire coupling) could be as large as half of C_{MOS} (~68.8 fF). In this paper, we focus on the calculation of the electrostatic capacitances. After this is accomplished, together with the C_{MOS} obtained by the method in [3], a complete resistance and capacitance (RC) circuit model can be built for a TSV structure. This can be extended to more general cases, such as that including MIVs.

The topology of MIVs and wires in monolithic 3-D IC is similar to that of TSVs and wires shown in Fig. 1. The difference is that MIVs have much smaller size and much larger density as well [5]–[7]. The diameter of MIV is similar to that of local via. However, since MIV passes through the device layer and interlayer dielectric (ILD), it has larger aspect ratio. Therefore, it is more important to accurately extract the MIVs capacitance than that of local via (sometimes ignored).

To sum up, we find out that accurately calculating the electrostatic capacitances of TSV/MIV in 3-D IC is important, and very few works have considered it. Furthermore, no one considers the 3-D cylinder shape of these ITVs while calculating electrostatic capacitances. To evaluate the effect of the square approximation [4] on the extracted ITV capacitances, we have simulated three typical TSV and MIV structures. The TSV-first structure is a "TSVs with top and bottom neighbors" structure, while TSV-last is a "TSVs with top, bottom, and side neighbors" structure, both obtained from [4]. We assume an equivalent single-dielectric environment in this experiment, as in [4]. And, the dielectric permittivity is set to 1. The side view and top view of the TSV-last structure are shown in Fig. 3, with detailed parameters in Table I. The keep-out-zone distance of TSV is set to 0.5 μm. In the MIV structure, a MIV is surrounded by a compact hexagon array of MIVs. The wire width equals to MIV diameter, and only three parallel wires are above or below the MIV array. The simulation has been performed with Synopsys Raphael [13]. In Raphael, a finite difference solver (RC3) with advanced nonuniform meshing scheme is employed. The result of Raphael under very dense mesh is widely regarded as the golden value. Because the

TABLE I
CAPACITANCE RESULTS FROM THE REAL-CYLINDER MODEL AND AN APPROXIMATE SQUARE-SHAPE MODEL FOR THREE ITV STRUCTURES

Structure	Dimensions(μm)					C_{total} (aF)		Err. C_{total}	Error of C_{couple} (%)		
	TSV/MIV			Wire							
	D	h	s	w	t	Cylinder	Square	(%)	min	max	avg*
TSV-first	5	50	5	0.2	0.36	3740	3962	**5.9**	**-20**	**21**	**6.3**
TSV-last	5	50	5	0.2	0.36	3866	4065	**5.2**	**-38**	**71**	**13**
MIV	0.07	0.25	0.07	0.07	0.14	14.7	15.8	**7.5**	**-1.6**	**9.1**	**4.8**

* The average of the absolute values.

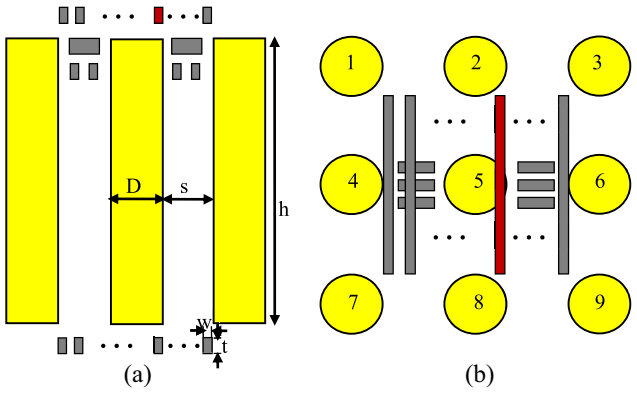

Fig. 3. Simulated TSV-last structure. (a) Side view. (b) Top view.

Neumann condition is assumed in Raphael for the outer boundary, a suitable large simulation boundary has been set to imitate the situation where the ground is at the infinity. We also set different grid numbers in Raphael for obtaining converged capacitance result for comparison shown in Table I. This is especially important for simulating the cylinder ITV cases, and guarantees the fidelity of the experiments. In the experiments, square approximation of an ITV is obtained by changing its circular cross section to a square with same area (i.e., square-edge size $a = \sqrt{\pi}D/2$). The capacitances related to the center ITV are extracted. Except for the square approximation with $a = \sqrt{\pi}D/2$, we have also tested other schemes of square approximation. If the cylinder is approximated by its bounding box (i.e., $a = D$), the capacitances would be largely overestimated. If the cylinder is approximated by its inscribed square block (i.e., $a = \sqrt{2}D/2$), our experiments also demonstrated that the capacitances could be underestimated by more than 20%.

From Table I, we can see that the square approximation overestimates the total capacitance by more than 5%. The error of coupling capacitances is much larger, often more than 20%. This verifies the necessity of modeling the ITV cylinders.

B. Floating Random Walk Method

The FRW method for calculating electrostatic capacitance is originated from expressing the electric potential of a point $\boldsymbol{r}$ as an integral of the potential on surface S enclosing $\boldsymbol{r}$ [11], [14]

$$\phi(\boldsymbol{r}) = \oint_S P\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right)\phi\left(\boldsymbol{r}^{(1)}\right)d\boldsymbol{r}^{(1)} \tag{1}$$

where $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is called surface Green's function. The domain enclosed by S is often called the transition domain. $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is non-negative for any point $\boldsymbol{r}^{(1)}$ on S, and can be regarded as

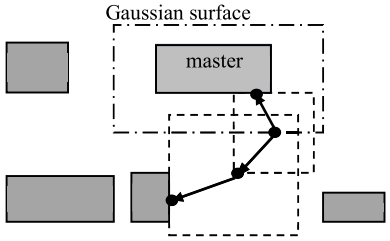

Fig. 4. Two examples of random walk in the FRW method for capacitance extraction (a 2-D top view).

the probability density function for selecting a random point on S. Therefore, $\phi(\boldsymbol{r})$ is the statistical mean of $\phi(\boldsymbol{r}^{(1)})$, and can be calculated with a Monte Carlo (MC) procedure.

To calculate the capacitances related to master conductor i, a Gaussian surface G_i is constructed to enclose it (see Fig. 4). According to the Gauss theorem, the charge of conductor i

$$Q_i = \oint_{G_i} F(\boldsymbol{r}) g \int_{S^{(1)}} \omega\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) q\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r} \quad (2)$$

where $F(\boldsymbol{r})$ is the dielectric permittivity at point $\boldsymbol{r}$, $q(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is the probability density function for sampling on $S^{(1)}$ which may be different from $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$, and $\omega(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is the weight value [11]. Thus, Q_i can be estimated as the statistical mean of sampled values on G_i, which is further the mean of sampled potentials on $S^{(1)}$ multiplying the weight value. If the sampled potential is unknown, the construction of transition domain and the spatial sampling procedure will repeat until a point with known potential is obtained (e.g., on conductor surface). This forms an FRW including a sequence of hops (see Fig. 4). Each hop is from the center of a transition domain to its boundary. With a number of such walks, the statistical mean of the weight values for the walks terminating at conductor j approximates the capacitance C_{ij} between conductors i and j (if $j \neq i$), or the total capacitance C_{ii} of master conductor i.

Although the surface Green's function for a spherical transition domain has simple analytical expression, the cubic transition domain is widely adopted because it well fits the Manhattan-shaped interconnects in very large-scale integration (VLSI) circuit [11]. This means larger probability for terminating a walk earlier. The sampling probability and weigh value for a cube domain can be precalculated and tabulated, so as to accelerate the sampling operation. Another technique is the space management [11], [12], which largely facilitates finding the nearest conductor for constructing the transition cube, especially for large structure.

The total runtime of the FRW method is roughly

$$T_{\text{total}} = N_{\text{walk}} \cdot N_{\text{hop}} \cdot T_{\text{hop}} \quad (3)$$

where N_{walk} is the number of random walks, N_{hop} is the average number of hops per walk, and T_{hop} is the average computing time for a hop. The variance reduction techniques in [11] contributes to the reduction of N_{walk}, while suitable transition domains and efficient space management approach are crucial to the reduction of N_{hop} and T_{hop}, respectively.

C. Variance Reduction Techniques for the FRW Method

The fast FRW algorithm [11] relies on an efficient variance reduction approach [including the importance sampling and stratified sampling (SS)], which accelerates the MC convergence rate for various structures. Below, we briefly review the variance reduction approach used in [11].

Based on the idea of SS, the integral domains in (2) is divided into strata. The Gaussian surface G_i is decomposed into its n_g faces, and the surface of the first transition cube $S^{(1)}$ is divided into two parts, standing for the halves outside and inside the Gaussian surface, respectively. Now, (2) is converted into

$$\begin{aligned} Q_i = &\sum_{k=1}^{n_g} \int_{\Gamma_{i,k}} F(\boldsymbol{r}) g \int_{S_a^{(1)}} \omega\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) q\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r} \\ &+ \sum_{k=1}^{n_g} \int_{\Gamma_{i,k}} F(\boldsymbol{r}) g \int_{S_b^{(1)}} \omega\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) q\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r} \end{aligned} \quad (4)$$

where $\Gamma_{i,k}$ is the kth face of G_i, and the constant g satisfies $\oint_{G_j} F(\boldsymbol{r}) g d\boldsymbol{r} = 1$. This means the integral for Q_i becomes the sum of integrals on $2n_g$ strata, each of which is calculated independently and through the FRW procedure. Taking one stratum as an example, the corresponding integral is [11]

$$\begin{aligned} I_k = A_k \int_{\Gamma_{j,k}} \frac{F(\boldsymbol{r}) g}{A_k} \int_{S_a} \\ -\frac{K_a}{gL(\boldsymbol{r})} q_a\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r}, \ (1 \leq k \leq ng) \end{aligned} \quad (5)$$

where $A_k = \int_{\Gamma_{j,k}} F(\boldsymbol{r}) g d\boldsymbol{r}$ and S_a is a half of the surface of a unit-size cube. K_a is a constant, $q_a(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is a probability density function for sampling on surface S_a, and $L(\boldsymbol{r})$ is the edge size of the first transition cube. Note that in (5) the second integral is calculated on the surface of a unit-size cube, and both K_a and $q_a(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ are independent of the first transition cube.

Equation (5) can be interpreted by an FRW procedure, where sampling on S_a obeys the probability function of $q_a(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ and the corresponding weight value is

$$\omega_a\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) = -\frac{K_a}{gL(\boldsymbol{r})}. \quad (6)$$

For the transition cubes with same size and dielectric configuration, the weight value is constant. Thus, the variance of the FRW procedure can be largely reduced, resulting in the acceleration of convergence for a given accuracy criterion.

III. FRW-Based Techniques for Extracting the Capacitances of Structure With Cylindrical ITVs

In this section, we first present an extension of the FRW method to handle the cylindrical ITVs. Then, the technique which rotates the Manhattan transition cubes to reduce the number of hops is proposed. Finally, the problem of accelerating each hop for structures with a large number of ITVs is considered, followed by algorithm description and some discussions.

A. Walk With Manhattan Transition Cubes

Since the FRW method has very high efficiency to handle Manhattan geometries, a straightforward idea is still using "Manhattan" transition cubes but treating the ITV

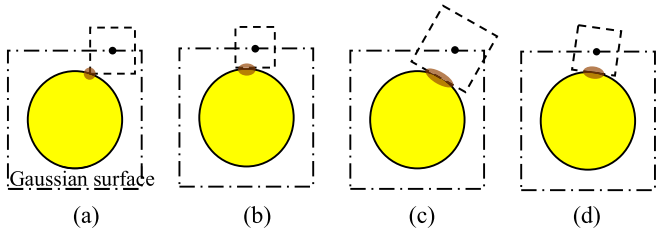

Fig. 5. 2-D topologies of a cylindrical ITV and (a) and (b) Manhattan transition cube or (c) and (d) rotated transition cube.

cylinder exactly. Here, "Manhattan" refers to a shape with each surface parallel to one of the *xoy*, *yoz*, and *zox* axis planes. We call this FRW-1 method, which is a simple extension of the original FRW method.

For each hop of random walk, a maximum transition cube which does not intersect any conductor is needed. As in existing works, with the space management technique it is easy to find the nearest Manhattan conductor block. The ∞-norm distance between the current point of walk and the nearest block is the half edge size of a transition cube. However, this cube may intersect the cylinders and becomes invalid. To avoid this, we can further check all cylinders one by one, and shrink the cube once it crosses a cylinder. After that, we obtain the transition cube for performing an FRW hop.

Below, we show how to calculate the size of the valid transition cube while taking an ITV cylinder as the obstacle. Without loss of generality, we assume the cylinder's center is at (0, 0, 0), its diameter and height are D and h, respectively. The current position of walk is (x, y, z). A vertical distance and a horizontal distance are calculated separately. And, the larger one of them is the half edge size of the Manhattan transition cube.

First, it is easy to see that the vertical distance is

$$d_v = |z| - h/2. \tag{7}$$

To calculate the horizontal distance we look at the 2-D top view of a cylinder and a cube (i.e., a circle and a square). Two situations are shown in Fig. 5(a) and (b). If $-D/2 = |x|-|y| \le D/2$, as in Fig. 5(a), only a corner of the square touches the circle. The half edge size of the square, i.e., the horizontal distance d, fulfills

$$(|x| - d)^2 + (|y| - d)^2 = D^2/4 \tag{8}$$

whose meaningful solution is

$$d = \left(|x| + |y| - \sqrt{D^2/2 - (|x| - |y|)^2}\right) \Big/ 2. \tag{9}$$

Otherwise, i.e., the situation shown in Fig. 5(b), the square touches the circle at an inner point of edge. In this case

$$d = \max(|x|, |y|) - D/2. \tag{10}$$

Combining (9) and (10), we get the horizontal distance d_{h1}

$$d_{h1} = \begin{cases} \max(|x|, |y|) - D/2, & ||x| - |y|| > D/2 \\ \left(|x| + |y| - \sqrt{D^2/2 - (|x| - |y|)^2}\right) \Big/ 2, & ||x| - |y|| \le D/2. \end{cases} \tag{11}$$

Therefore

$$d_1 = \max(d_v, d_{h1}) \tag{12}$$

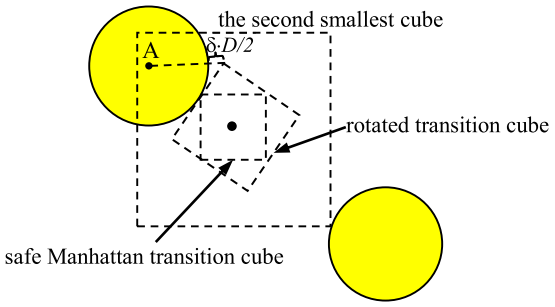

Fig. 6. Rotated transition cube is a better choice.

is the half edge size of the transition cube considering a specific cylindrical ITV.

In Fig. 5(a) and (b), we use green shadow to indicate the contact between the cylinder and the Manhattan transition cube. Its size is so small, if comparing with that in Fig. 4. Therefore, the random walk using Manhattan transition cube has less probability to terminate quickly, and is thus inefficient.

B. Walk With Rotated Transition Cubes

The FRW-1 method can be improved by allowing the transition cube to rotate in the *xoy* plane. This brings better touch to the cylinder [see Fig. 5(c) and (d)]. It increases the probability of terminating a walk, and reduces the number of hops. With this strategy, the horizontal distance for calculating the half edge size of the transition cube can be

$$d_{h2} = \sqrt{x^2 + y^2} - D/2 \tag{13}$$

which is not less than d_{h1} in (11). However, the rotated transition cube may intersect other conductor, which is forbidden.

By traversing all the cylinders one by one and repeatedly calculating with (12), we get the final (also the smallest) Manhattan transition cube for performing an FRW hop. Suppose the final cube's size is limited by cylinder A. During this course, we can also get the second smallest transition cube which only intersects A. If the rotated transition cube with the half edge size calculated with (13) is inside the second smallest cube (see Fig. 6), it certainly will not intersect any other conductor, and therefore should be accepted. Otherwise, we shall still use the Manhattan transition cube.

A δ-touching criterion can be used to terminate a walk close to an ITV cylinder. That is, if the distance between the current position and a cylindrical surface is no more than $\delta \cdot D/2$ (δ is a small quantity), we regard that the walk has reached the cylinder. If the rotated transition cube is used, this can be applied more efficiently. We can calculate the largest distance from the cube's touching face to the cylinder. If it is no more than $\delta \cdot D/2$ (equivalently $d_{h2} \le D/2 \cdot \sqrt{\delta(2+\delta)}$), any hop to that face makes the walk terminated, which has a fixed 1/6 probability. Now, we get a method with rotated transition cubes (called FRW-2).

The δ-touching criterion introduces some error, and affects the efficiency of the proposed approach. In [19] and [30], the influence of δ has been studied for a similar random walk approach with spherical transition domains. It is revealed that the error caused by the δ-touching is linear in δ, while the runtime is about $O(-\ln(\delta))$. This means that we can easily make the error caused δ-touching smaller than the statistical error, and the runtime of the proposed approach increases slowly as

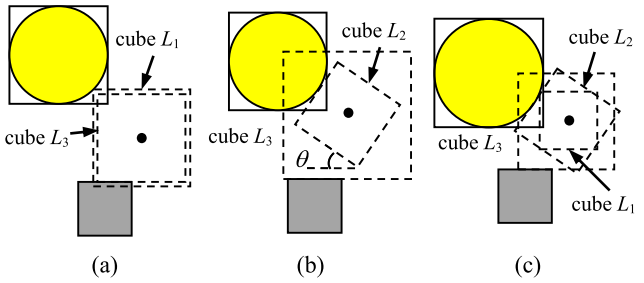

Fig. 7. Construct transition domain according to the nearest cylinder and the second nearest block. (a) Manhattan transition cube touching cylinder (L_1) is larger than the transition cube touching the second nearest block (L_3). (b) Rotated transition cube (L_2) is within transition cube L_3. (c) L_2 exceeds the boundary of transition cube L_3.

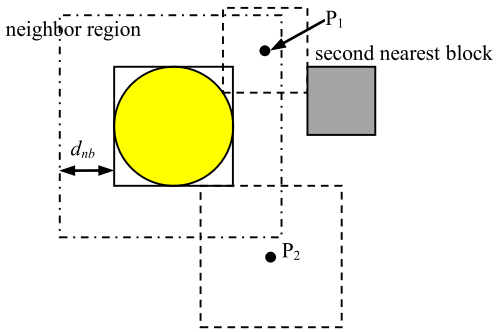

Fig. 8. Cylindrical ITVs neighbor region.

δ decreases. In this paper, we set δ to 5×10^{-4}, which makes the induced error negligible for the numerical experiments.

In FRW-2 method, we traverse all cylindrical ITVs in each hop. If there are many ITVs in the extracted structure, the time for performing a hop will be very large, which greatly harms the runtime of the algorithm.

C. Reduce the Time for Each Hop

To reduce the average computing time for a hop for the situation where a large number of cylindrical ITVs are involved, we consider the space management technique. First, we can insert each ITVs Manhattan bounding box into the space management structure [11]. This does not induce any modification of the existing approach. Therefore, we can easily find the nearest block from current walking point. This block is either a regular conductor or an ITVs bounding box. If it is the former, the transition cube is constructed normally. For the latter case, we have to consider the ITV cylinder and perform further computation.

When the nearest block is an ITVs bounding box, we may be able to find a larger transition domain touching the ITVs cylinder. According to (11) and (13), we can construct two transition cubes touching the ITVs cylindrical surface with edge sizes L_1 and L_2, respectively. Obviously, $L_2 \geq L_1$. However, the both may not be safe (may intersect other conductor). To ensure this safety, we can find the second nearest conductor block and construct a Manhattan transition cube (with size L_3) touching it. It does not matter if the block is an ITVs bounding box. We now choose one from the three transition cubes. If $L_3 < L_1$, we have to choose the third transition cube to avoid intersecting any conductor [see Fig. 7(a)]. Otherwise, we judge the condition $(|\cos(\theta)| + |\sin(\theta)|)L_2 \leq L_3$, where θ is the rotation angle of the rotated transition cube. If the condition satisfies, we can choose the second transition cube (with size L_2) which is inside the third one and is safe [see Fig. 7(b)]. If the condition does not stand, it is not guaranteed that the rotated transition cube is safe. To exactly judge whether the rotated transition cube intersects other conductors would involve a lot of computation. Therefore, we just choose the safe first transition cube with size L_1. This situation is shown in Fig. 7(c). Note in each of the three situations, the transition cube really touches a conductor body instead of ITVs bounding box. And, if the size of the chosen transition cube is zero, the current point must be on the cylindrical surface and we shall terminate the walk.

The left problem is how to find the second nearest block without traversing conductor blocks one by one. We can define each ITVs neighbor region by expanding a distance d_{nb} based on its bounding box (see Fig. 8). In the initialization of the space management data structure [12], we treat ITVs neighbor region as a special spatial cell and generate a candidate list containing the possible nearest blocks from any points in the cell. The only difference is that the ITV itself is not inserted into the candidate list. During the hop, when current point's nearest block is an ITVs bounding box, we first check if it is in the ITVs neighbor region. If it is (see point P_1 in Fig. 8), we can easily get the second nearest block with a precalculated candidate list. However, if the point is out of the neighbor region (see point P_2 in Fig. 8) the second nearest block cannot be found. In this situation, we just use the Manhattan transition cube restricted by the ITVs bounding box, whose half edge size is larger than d_{nb}. By setting a suitably large d_{nb}, it is guaranteed that we either get the second nearest block efficiently or use a large enough transition cube. This largely reduces the time of performing a hop while handling the structure with a large number of cylindrical ITVs.

D. Algorithm Flow and Discussion

With the technique in the last section, we obtain method FRW-3 for extracting the capacitances for a structure with cylindrical ITVs. With this method, the flow of performing an FRW walk can be described as the following Algorithm 1.

The function $d(\ ,\ )$ in steps 2 and 7 calculates the ∞-norm distance between a point and a 3-D Manhattan block. Steps 11 and 12 determine a rotated transition cube.

A whole description of FRW-3 is given as Algorithm 2.

In the FRW-3 algorithm, no assumption of the number, size, and positions of ITVs is made. We only assume that the Manhattan bounding box of an ITV does not intersect other conductor block or ITVs bounding box. In realistic layouts, this is obviously satisfied. Because of the importance sampling function $q(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ used for the integral on the first transition cube [11], the first transition cube must be of "Manhattan" type. In step 6 of Algorithm 2, we do not rotate the transition cube.

As described in Section III-C and Algorithm 1, the FRW-3 method performs extra computation for generating rotated transition cube only when the current point is close to an ITV. The space management is also a small modification of the existing techniques [11], [12]. Therefore, the increase of computational cost should be limited as compared with the original FRW algorithm which only handles Manhattan objects.

Because the cubic transition domains are still used, the proposed method can be easily extended to the problem with

Algorithm 1 FRW Walk in the FRW-3 Method (Startpoint P)

B := the nearest conductor block (or ITV bounding box) from P;
d := d(P, B); *IsRotated* := false;
If B isn't an ITVs bounding box **then goto** Step 16; **Endif**
Use V to denote the cylindrical ITV inside B;
If d > ITVs d_{nb} **then goto** Step 16; **Endif**
d := d_1(P, V); // calculate with (12) in **FRW-1**.
S := d(P, the nearest block found from V's candidate list);
If S < d **then**
  d := S; **goto** Step 16;
Endif
L := $d_{h2}(P, V)$; // calculate with (13).
Get θ, which is the rotation angle of the transition cube;
If d < L and $(|\cos(\theta)| + |\sin(\theta)|)$L < S **then**
  d := L; *IsRotated* := true;
Endif
If d < a small tolerance **then**
  This walk terminates at conductor B or V; **return.**
Endif
Use d as the half edge size to construct a Manhattan transition cube;
If *IsRotated*, **then** rotate the transition cube by θ; **Endif**
P := a randomly selected point on the transition cube;
goto Step 1;

Algorithm 2 FRW-3 Algorithm for Structure With Cylindrical ITVs

Load pre-computed transition probabilities and weight values;
Construct the Gaussian surface enclosing master conductor i;
C_{ij} :=0, $\forall j$; *npath* := 0;
Repeat
  npath: = *npath*+1;
  Pick a point $\boldsymbol{r}$ on the Gaussian surface, and generate a cubic transition domain S centered at $\boldsymbol{r}$; pick a point $\boldsymbol{r}^{(1)}$ on the surface of S with the transition probabilities and then calculate the weight value ω with the pre-computed data;
  Perform a walk starting from $\boldsymbol{r}^{(1)}$; //Algorithm 1
  C_{ij} := C_{ij} +ω; //the walk terminates at conductor j
Until the convergence criterion is met
C_{ij} := C_{ij} /*npath*, $\forall j$.

multilayered dielectrics. It can be accomplished by plugging in the precharacterized multidielectric surface Green's function and weight value tables as [11].

IV. Accelerating the FRW Procedure for Structures Including TSVs

Because the TSVs have much larger dimensions than conventional interconnect wires, some strategies in the existing FRW solvers [11], [12] may not be suitable. In this section, the specific techniques of the Gaussian surface construction and the MC variance reduction are proposed to accelerate the FRW procedure for extracting capacitances of the structures with TSVs.

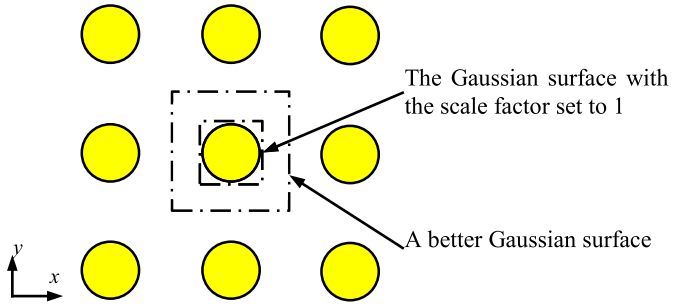

Fig. 9. Top view of the TSV-first structure and Gaussian surfaces.

A. Construction of Gaussian Surface Around TSV

In the FRW-based capacitance extraction, the random walks start from the Gaussian surface surrounding the master conductor. The placement of Gaussian surface has an impact on the runtime of the FRW algorithm.

One can describe the placement of a Gaussian surface with the six distances between it and the enclosed conductor along six directions (i.e., PX, PY, PZ, NX, NY, and NZ). Here, PX and NX denote the positive and negative directions along the x-axis, respectively. The other four denotations are similarly defined. A general strategy to determine these distances is based on finding the equidistant positions between the master and its nearest neighbor conductor [20]. However, the distances corresponding to the equidistant positions cannot be directly used. To avoid large distance variance along the directions which may worsen the convergence behavior of the FRW procedure, the minimum of the six distances is multiplied by a scale factor to produce an allowable maximum distance. Then, this allowable maximum distance is used to limit the six distances to construct the Gaussian surface actually used.

The scale factor used in the construction of Gaussian surface is a key parameter. If it equals 1, the strategy is that used in [11]. In [20], a lot of experiments have been carried out for VLSI interconnect structures. The results show that with a scale factor slightly larger than 1 the Gaussian surface brings the best efficiency to the FRW-based capacitance extraction.

For extracting the capacitances related to a TSV, the existing approach to constructing the Gaussian surface also applies because TSVs bounding box is a Manhattan block and there is a keep-out zone around it. However, the distances from the master TSV to its neighbor conductors vary much along different directions. For example, the spacing between a TSV and its neighbor can be only 0.3 μm along the PZ and NZ directions, but 10 μm along lateral directions. If the scale factor equal to 1 is used to construct the Gaussian surface (see Fig. 9), it becomes very far from the adjacent TSVs. In most situations, this causes the first FRW transition cube much smaller than what it can be. Because the size of the first cube affects the variance of the weight values in random walks, and it is desirable to have larger first transition cube to reduce the number of walks for a given accuracy criterion [11], we shall set a large scale factor to get the better Gaussian surface (also shown in Fig. 9). This makes sure that in the PX, NX, PY, and NY directions the Gaussian surface is exactly at the equidistant positions between the master and its adjacent TSV.

To fit the characteristics of the structure with TSVs, another modification is made during the construction of the Gaussian surface. While finding the equidistant positions between the

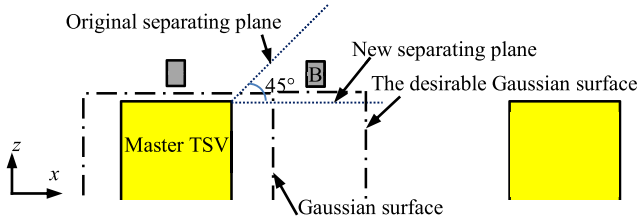

Fig. 10. Side view of the Gaussian surface for a TSV structure.

master and its nearest neighbors along the six directions, each environment conductor should be used for calculating the distance to the master along a certain direction. In existing FRW algorithms, all directions are treated equally. This means, for example, the conductor B in Fig. 10 is considered as an obstacle for calculating the distance along PX direction. This is because B is blow the 45° separating plane between PX-direction obstacles and PZ-direction obstacles. In this example, it is clear that the original treatment would make B limiting the PX-direction distance of the Gaussian surface. So, to produce the desirable Gaussian surface, we change the separating plane between PX-direction obstacles and PZ-direction obstacles to the horizontal plane shown in Fig. 10.

The above strategy for constructing the Gaussian surface for the cylindrical TSV takes the large dimensions of TSV into account, and makes the first transition cube as large as possible.

B. Optimized Importance Sampling Scheme

For the structure with TSVs and horizontal wires, the distance between the master TSV and its surrounding Gaussian surface would vary largely. Therefore, the size of the first transition cube [i.e., $L(\boldsymbol{r})$] has large variance. Usually, the $L(\boldsymbol{r})$ corresponding to the walks starting from the top or bottom faces of the Gaussian surface is much smaller [see Fig. 11(a)]. They cause larger variance of weight value and worsens the convergence rate of the FRW procedure. So, we propose an optimized importance sampling scheme to settle this issue.

Our idea is to apply the importance sampling to the first integral in each stratum's integral as well [see (4)]. Taking the integral on the kth stratum as an example, we have

$$I_k = A'_k g \int_{\Gamma_{j,k}} \frac{p(\boldsymbol{r})}{A'_k} \cdot \frac{F(\boldsymbol{r})}{p(\boldsymbol{r})} \int_{S_a} -\frac{K_a}{gL(\boldsymbol{r})} q_a\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r} \tag{14}$$

where $A'_k = \int_{\Gamma_{j,k}} p(\boldsymbol{r}) d\boldsymbol{r}$ and $p(\boldsymbol{r})$ has non-negative value for any $\boldsymbol{r}$ on $\Gamma_{i,k}$. In (14), $p(\boldsymbol{r})/A'_k$ is regarded as the probability density function for sampling on $\Gamma_{i,k}$. In the existing FRW solvers, $p(\boldsymbol{r}) = F(\boldsymbol{r})$ is assumed and has been verified to bring the best efficiency for the conventional VLSI interconnect structures [20]. To reduce the large variance caused by small values of $L(\boldsymbol{r})$, we should change $p(\boldsymbol{r})$ to sample more points on the portion of the Gaussian surface which produces small $L(\boldsymbol{r})$, for example its top face and bottom face.

Because the trend of $L(\boldsymbol{r})$'s value basically follows the distance from $\boldsymbol{r}$ to the TSVs surface, we set $p(\boldsymbol{r}) = F(\boldsymbol{r})/D(\boldsymbol{r})$, where $D(\boldsymbol{r})$ is the Euclidean distance of point $\boldsymbol{r}$ to the surface of TSV (see Fig. 11). Therefore, more samples are taken on

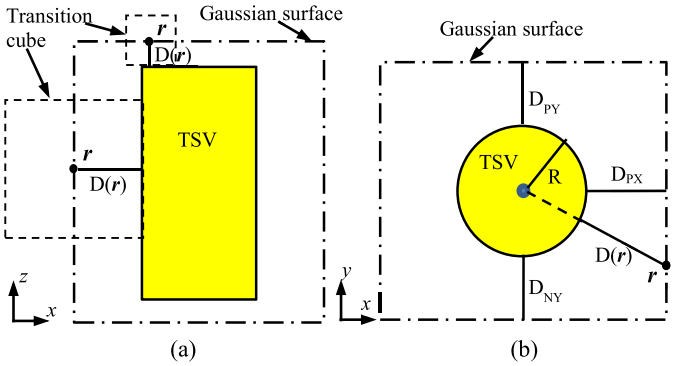

Fig. 11. $D(\boldsymbol{r})$ for different points on TSVs Gaussian surface. (a) Side view. (b) Top view.

the Gaussian surface's top and bottom faces, making the total variance reduced. Now, (14) becomes

$$I_k = A'_k g \int_{\Gamma_{j,k}} \frac{F(\boldsymbol{r})}{A'_k D(\boldsymbol{r})} \cdot D(\boldsymbol{r}) \int_{S_a} -\frac{K_a}{gL(\boldsymbol{r})} q_a\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) \phi\left(\boldsymbol{r}^{(1)}\right) d\boldsymbol{r}^{(1)} d\boldsymbol{r} \tag{15}$$

and

$$A'_k = \int_{\Gamma_{j,k}} \frac{F(\boldsymbol{r})}{D(\boldsymbol{r})} d\boldsymbol{r}. \tag{16}$$

The weight value for the FRW procedure calculating (15) is

$$\omega'_{a,k}\left(\boldsymbol{r}, \boldsymbol{r}^{(1)}\right) = -\frac{A'_k K_a D(\boldsymbol{r})}{L(\boldsymbol{r})} \tag{17}$$

whose value varies less globally.

The rationality of the importance sampling scheme shown in (15) can be explained in another way. Because we are calculating the electric charge (2), i.e., the integral of normal electric field intensity, the ideal importance sampling function should approximate the variance of the normal electric field intensity. In fact, $p(\boldsymbol{r}) = F(\boldsymbol{r})/D(\boldsymbol{r})$ reflects the decaying-with-distance property of electric field, and is therefore efficient for improving the convergence rate of the MC procedure.

Now, there are two problems. One is calculating A'_k with (16), and the other is sampling on $\Gamma_{i,k}$ with the probability function of $p(\boldsymbol{r})/A'_k$. The first one can be resolved with an analytical integration technique. Taking the side face in the PX direction as an example [see Fig. 11(b)]

$$A'_k = A_{PX} = \int_{z_{\min}}^{z_{\max}} \int_{y_{\min}}^{y_{\max}} \frac{F(y,z)}{D(y)} dydz. \tag{18}$$

$F(y,z)$ is the dielectric permittivity and we only consider the layered dielectric medium. This means $F(y,z)$ only depends on z. So

$$A_{PX} = \int_{z_{\min}}^{z_{\max}} F(z)dz \cdot \int_{y_{\min}}^{y_{\max}} \frac{1}{D(y)} dy \tag{19}$$

where the first integral can be easily calculated. Assuming the coordinate origin at the cylinder's center, we have the second integral

$$\int_{y_{\min}}^{y_{\max}} \frac{1}{D(y)} dy = \int_{-R-D_{NY}}^{R+D_{PY}} \frac{1}{\sqrt{y^2 + (R+D_{PX})^2} - R} dy \tag{20}$$

where R is the radius of TSV cylinder. The primitive function of function $1/(\sqrt{y^2+a}-1)$ is

$$H(y)=\ln(y+c)+\frac{\arctan\left(\frac{y}{\sqrt{a-1}}\right)+\arctan\left(\frac{y}{c\sqrt{a-1}}\right)}{\sqrt{a-1}} \quad (21)$$

where $c=\sqrt{y^2+a}$. Setting $a=(R+D_{PX})^2/R^2$, we obtain

$$\int_{y_{\min}}^{y_{\max}}\frac{1}{D(y)}dy=H\left(\frac{D_{PY}}{R}+1\right)-H\left(-\frac{D_{NY}}{R}-1\right). \quad (22)$$

With (19), (21) and (22), A_{PX} can be calculated. For A'_k corresponding to another side face, similar treatment applies.

Sampling on the Gaussian surface with the probability function of $p(\boldsymbol{r})/A'_k$ can be done with the rejection sampling technique [26]. Suppose, we have a value U that satisfies $U \geq p(\boldsymbol{r})=F(\boldsymbol{r})/D(\boldsymbol{r})$ for any point $\boldsymbol{r}$ on the integral domain. We first sample on the integral domain uniformly, and then only accept a sample with the probability $p(\boldsymbol{r})/U$. If a sample is rejected, we repeat the procedure until getting an acceptable one. In this way, the accepted samples follow the probability density function of $p(\boldsymbol{r})/A'_k$. Because sampling on the Gaussian surface costs a very small part of the time for executing the FRW algorithm, the overhead of the rejection sampling approach is negligible.

With the special Gaussian surface placement and the importance sampling technique, we obtain algorithm FRW-4, which is suitable for the structure with TSVs. FRW-4 has similar algorithm description to that of FRW-3 (Algorithm 2 in Section III-D), except that modification is made in step 2 and the weight values are collected for each stratum separately before calculating the capacitances and convergence criterion. For the structure with MIVs, the techniques in this section brings no benefit, because the geometry size of MIV is similar to that of conventional interconnect wires.

V. Discussion on Applying the Proposed Method to the Sign-Off Verification

In this paper, we consider the conductors in a net as a whole, and extract the capacitances related with the whole net. Note that there is no difficulty to handle a mixed structure of a cylindrical ITV connected with square landing pads. An efficient virtual Gaussian surface sampling technique has been proposed for a whole net which is a composition of blocks in different shapes [20]. It allows us to just construct the Gaussian surface for each conductor block individually, and makes it unnecessary calculating the envelope of the block's Gaussian surface for the whole net with complex geometry. This technique has been implemented in our program, as demonstrated in extracting the capacitances of a net including MIVs and horizontal wires in Section VI-B.

Now, we would like to discuss how the proposed method can be applied to the sign-off signal integrity analysis of IC interconnects.

Calculating the delay of a full signal path, for which the interconnect delay caused by parasitic RC is a dominant factor, is a critical task in digital circuit design. To achieve accuracy, all metal wires in a net should be segmented and converted to a distributed RC network with parasitic extraction techniques. Due to the simplicity of resistance calculation, the capacitance extraction is the major challenge. This distributed RC network is also required for the accurate crosstalk analysis and circuit simulation.

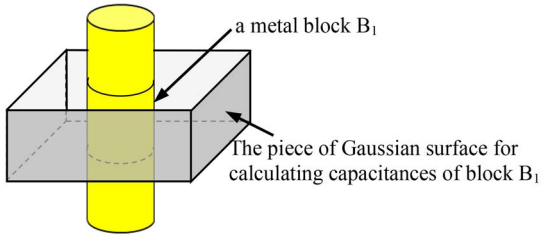

Fig. 12. Cylindrical TSV and a part of Gaussian surface enclosing it.

If using the FRW-based capacitance extraction tool, a simple approach for obtaining the distributed capacitances starts by performing the whole-net capacitance extraction. A Gaussian surface is constructed to enclose the whole net. Then, the wires in the net is segmented into blocks nominally and assigned a piece of surrounding Gaussian surface. Counting the walks starting from the piece of Gaussian surface for a block, we can get the capacitances related to the block (see Fig. 12). These capacitances of small metal blocks constitute the distributed capacitances.

The merit of this approach is that, both computation and error control are only made for the once extraction task. Actually, because the capacitances for a metal block is obtained from a smaller number of walks, the statistical error of FRW method for a block capacitance is larger than the specified error threshold for the whole-net capacitance. However, due to the statistical cancelation, the error of derived net delay would be comparable to the error associated with the whole-net total capacitance. An example in [28] has shown that the statistical error of Elmore delay is $\pm 2.3\%$, if the statistical error of whole-net total capacitance is controlled to $\pm 2\%$ in the FRW-based extraction. Therefore, setting a moderate accuracy criterion in the whole-net capacitance extraction can ensure the accuracy we need for the subsequent circuit analysis. As for the computational time, this approach is obviously superior to the approach extracting the capacitances of each metal blocks one by one.

VI. Numerical Results

We have implemented the proposed techniques based on RWCap [11]. The space management technique in Section III-C employs an octree structure and the pruning skills proposed in [12]. And, d_{nb} for the ITVs neighbor region is set to the radius of ITV. Several 3-D IC structures have been tested. We first use small and medium test cases to validate the accuracy and efficiency of the proposed method. Raphael [13] with dense grid discretization is used to validate the accuracy, and RWCap [11], [12] which only handles Manhattan geometries is compared. Then, the efficiency of the proposed space management technique and the accelerating techniques for TSV structures are demonstrated in two sections, with more test cases. Finally, we validate the versatility of the proposed techniques with multidielectric cases. The results of two fast BEM solvers, i.e., FastCap [15] and QBEM [16], are also presented for comparison.

Experiments are carried out on a Linux server with Intel Xeon E5-2650 2.0 GHz CPU. All results are obtained from the execution of serial computing.

TABLE II
RESULTS OBTAINED FROM EXTRACTING AN ITVS TOTAL CAPACITANCE (IN UNIT OF aF)

Case	Raphael			RWCap		FRW-4		
	cylinder	square	Err(%)	C_{tot}	Time(s)	C_{tot}	Err(%)	Time(s)
TSV-first	3740	3962	**5.9**	3930	2.06	3793	**1.4**	1.66
TSV-last	3866	4065	**5.1**	4056	2.01	3885	**0.5**	2.79
MIV	14.7	15.8	**7.5**	15.6	0.61	14.8	**0.7**	1.88
TSV-first2	3718	3939	**5.9**	3916	2.58	3747	**0.8**	1.90

TABLE III
RESULTS OBTAINED FROM EXTRACTING AN ITV RELATED COUPLING CAPACITANCE (IN UNIT OF aF)

Case	Raphael			RWCap		FRW-4		
	cylinder	square	Err(%)	C_c	Time(s)	C_c	Err(%)	Time(s)
TSV-first	49.9	60.2	**20.6**	59.6	3.5	50.0	**0.2**	4.22
TSV-last	48.2	58.6	**21.6**	58.2	4.2	47.9	**-0.6**	5.11
MIV	2.06	2.24	**8.7**	2.26	2.6	2.12	**2.9**	6.83
TSV-first2	50	60.4	**20.8**	60.0	3.9	49.7	**-0.6**	4.61

A. Results for Small and Medium Cases

Four structures are tested, and three of them are those described in Table I. The last one "TSV-first2" is the same as "TSV-first," except that TSVs nos. 1, 3, 7, and 9 and several horizontal wires are removed (see Fig. 3). For each case, the total capacitance of the center ITV is first extracted. The results obtained with Raphael, RWCap, and our FRW method (setting 1-σ error to be 0.5% of the mean value) are listed in Table II. From it we see that the discrepancy between the result of our method and the Raphael's result got from accurately modeling cylinder shape is within 1.5%. The result of RWCap is close to the Raphael's result based on the square approximation, which exhibits from 5.1% to 7.5% error on the total capacitance of ITV. While comparing the runtime of RWCap and the proposed method (FRW-4), we see that for the TSV cases the latter consumes less or similar time. For the MIV case, the proposed method is about 3× slower than RWCap.

To evaluate the accuracy of the proposed method for extracting coupling capacitance, we present a result in Table III. For the TSV structures, it is the coupling capacitance between the center TSV and a horizontal wire (the red one in Fig. 3), while for the MIV structure it is the coupling between the center MIV and a neighbor MIV. When running the FRW algorithms, we set the horizontal wire as the master conductor and the 1-σ error of the coupling capacitance to 1% of its mean value for termination. From Table III, we can see the large error brought by the square-shape approximation (over 20% error in the TSV cases, and 8.7% error in the MIV case). And, the proposed method exhibits high accuracy in comparison with Raphael's result with cylinder model. For the runtime, the proposed method only increases 20% computing time of that consumed by RWCap for the TSV structures. This runtime overhead of the proposed method is moderate.

FastCap and QBEM are also run with the ITV and the horizontal wire set as the master conductor, respectively. Their computational results are listed in Tables IV and V. To make the computation feasible, each cylinder is approximated by a regular 16-side prism and the cylindrical surface is replaced by 16 rectangles. The approximation with regular 32-side prisms has also been tried, which produces similar results. In the tables, "Err" denotes the error measured according to Raphael's result. We can see that FastCap has good accuracy on the total capacitance, but is quite inaccurate on the TSV related coupling capacitance (see Table V). Note in these cases, there are TSVs with large dimensions and a number of horizontal wires. So, the panel discretization employed in FastCap may not dense enough for producing accurate coupling capacitance. We have tried denser discretization, but FastCap broke down due to its limitation of 2 GB memory usage. On the other hand, QBEM employs an automatic boundary discretization and is able to extract the total and coupling capacitances to certain accuracy. The error of QBEMs result may be due to the 16-side prism approximation and the imperfect quality of boundary discretization mesh.

From the tables, we see that the FRW-4 algorithm consumes comparable or more time than the fast BEM solvers while extracting the capacitance of the small MIV case. However, for the TSV cases, our algorithm is more than 10×, and up to 242× faster while extracting the total and coupling capacitances accurately. Generally, the runtime speedup of the FRW-based method increases with increased size of test case. In Tables IV and V, we have also listed the results obtained with FRW-1 algorithm, which is a simple extension of the original FRW method. Compared with FRW-1, the FRW-4 algorithm is more than 10× faster for extracting TSVs total capacitance. For extracting the coupling capacitances, this speedup ratio is about 1.3. It is because the horizontal wire is set as the master conductor, and fewer random walks go to the neighborhood of ITVs. From the data in Tables II–V, we also see that the accuracy of FRW-1 and FRW-4 algorithms is not distinguishable.

For the test cases with the single dielectric assumption, the memory cost of our FRW algorithms is no more than 1MB. It is negligible if compared with the memory needed by the BEM solvers (see Tables IV and V).

B. Results for Large Cases

To test the proposed techniques for large-scale structures, four large cases with more ITVs are constructed.

1) *viafirst100:* A random placement of 100 TSVs of diameter 4 μm and height 40 μm, plus a top and bottom layers of parallel wires (see Fig. 13). The wire dimensions follow those in case TSV-first; the spacing between any two TSVs is kept to be larger than 4 μm.
2) *viafirst400:* The structure is similar to that of viafirst100, except that the random TSV placement includes 400 TSVs.
3) *MIV144:* A regular layout of transistor-level monolithic 3-D IC, with 144 MIVs (see Fig. 14). The dimensions of MIV and wires are the same as those in case MIV. There are parallel wires in the very top and bottom metal layers.
4) *MIV576:* Formed by duplicating case MIV144 for four times.

Thus, we have totally eight test cases. The number of ITVs and the number of conductor blocks (for wires) in each test case are listed in Table VI. For the large cases with at least 100 cylindrical ITVs and 350 wires, it becomes infeasible to simulate them with Raphael. The FastCap program [15] has a limitation of 2 GB memory usage, and is not workable either.

TABLE IV
COMPARISON OF THE FAST BEM SOLVERS AND OUR METHODS FOR THE TOTAL-CAPACITANCE EXTRACTION

Case	FastCap					QBEM					FRW-1		FRW-4				
	C_{tot}(aF)	Err(%)	#panel	Time(s)	Mem.	C_{tot}(aF)	Err(%)	#panel	Time(s)	Mem.	C_{tot}(aF)	Time(s)	Time(s)	Sp1*	Sp2*	Sp3*	Mem.
TSV-first	3710	-0.8	190K	67.3	1.8GB	3603	-3.7	118K	402	7.6GB	3796	42.0	1.66	**40**	**242**	**25**	~1MB
TSV-last	3736	-3.4	197K	79.0	1.9GB	3708	-4.1	118K	404	7.7GB	3904	36.1	2.79	**28**	**145**	**13**	~1MB
MIV	14.7	0.0	40K	8.43	407MB	14.33	-2.5	6.5K	1.58	48MB	14.85	2.08	1.88	**4.5**	**<1**	**1.1**	<1MB
TSV-first2	3691	-0.7	117K	50.1	1.1GB	3547	-4.6	82K	271	5.3GB	3783	35.3	1.90	**26**	**143**	**19**	~1MB

*Sp1, Sp2 and Sp3 are the speedup ratios to FastCap, QBEM and FRW-1, respectively.

TABLE V
COMPARISON OF THE FAST BEM SOLVERS AND OUR METHODS FOR THE COUPLING-CAPACITANCE EXTRACTION

Case	FastCap					QBEM					FRW-1		FRW-4				
	C_c(aF)	Err(%)	#panel	Time(s)	Mem.	C_c(aF)	Err(%)	#panel	Time(s)	Mem.	C_c(aF)	Time(s)	Time(s)	Sp1*	Sp2*	Sp3*	Mem.
TSV-first	64.9	**30.1**	190K	66.8	1.8GB	48.0	-3.8	109K	298	5.9GB	49.8	6.07	4.22	**18**	**71**	**1.4**	~1MB
TSV-last	64.5	**33.8**	197K	79.1	1.9GB	46.1	-4.4	110K	299	6.0GB	48.4	6.55	5.11	**16**	**59**	**1.3**	~1MB
MIV	2.11	2.4	40K	8.23	407MB	2.06	0.0	6.5K	1.58	48MB	2.13	7.00	6.83	**1.2**	**<1**	**1.0**	<1MB
TSV-first2	65.1	**30.3**	117K	51.2	1.1GB	47.9	-4.2	85K	192	4.2GB	49.8	5.23	4.61	**11**	**42**	**1.1**	~1MB

*Sp1, Sp2 and Sp3 are the speedup ratios to FastCap, QBEM and FRW-1, respectively.

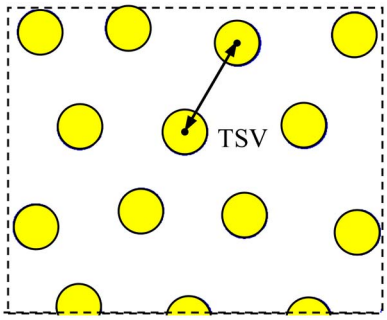

Fig. 13. Part of 2-D top view of TSVs in case viafirst100.

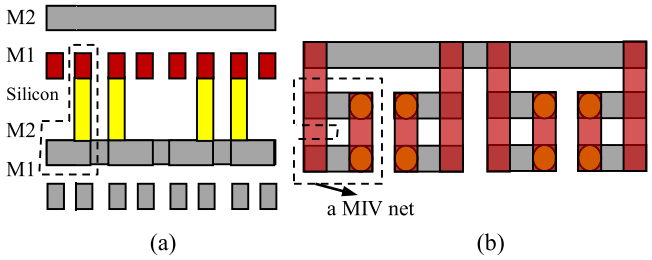

Fig. 14. Structure of MIV144 case. (a) Side view. (b) Top view of a small part of layout with eight MIVs (the parallel wires in the very top and bottom layers are not drawn).

TABLE VI
NUMBER OF ITVS AND CONDUCTOR BLOCKS IN EACH TEST CASE

Case name	# ITVs	# conductor blocks
MIV	7	6
TSV-first	9	74
TSV-first2	5	70
TSV-last	9	120
MIV144	144	350
MIV576	576	1400
Viafirst100	100	1705
Viafirst400	400	3681

TABLE VII
RESULTS OF QBEM AND THE PROPOSED FRW METHOD FOR EXTRACTING LARGE CASES

Case	QBEM					FRW-4			
	C_{tot}(fF)	Dis.(%)	#panel	Mem.	Time(s)	C_{tot}(fF)	Mem.	Time(s)	Sp.
MIV144	0.509	-5.9	27K	549MB	25	0.539	1MB	1.4	**18**
MIV576	0.515	-5.0	78K	5.2GB	270	0.542	3MB	1.4	**192**
Viafirst100	--	--	--	--	--	3.12	7MB	2.6	--
Viafirst400	--	--	--	--	--	3.03	29MB	3.1	--

For each of the four large cases, we set a net of ITV as the master conductor and extract the capacitances (a MIV net is outlined in Fig. 14). The results of QBEM and our FRW method are given in Table VII, where QBEMs results for the two largest cases are not available due to the issue of memory overflow. From Table VII, we can see that the proposed method can be up to 192× faster than QBEM for the large MIV case. The capacitance results of both methods are comparable. While comparing Table VII with Table III, we see that the proposed method costs less time for the large cases.

With these large cases, we demonstrate the individual effect of the techniques proposed in Section III. That means, we compare the simply extended FRW using Manhattan transition cube (FRW-1), the FRW using rotated transition cubes (FRW-2), and the FRW using both rotated transition cubes and the special space management (FRW-3). Their results are listed in Table VIII. Comparing FRW-1 and FRW-2, we see that with the rotated transition cubes the number of hops (N_{hop}) is reduced, which makes more than 2× speedup over FRW-1 for the TSV cases. And, FRW-3 is much faster than FRW-2, because with the space management the time for performing a hop can be largely reduced. For the largest case, the both techniques contribute 20× speedup totally.

C. Acceleration for the TSV Cases

To validate the efficiency of the techniques proposed in Section IV for the TSV structures, we compare FRW-4 and FRW-3 with the center TSV set as the master in each case. The results are listed in Table IX. "GSP" denotes the FRW-3 algorithm plus the Gaussian surface placement in Section IV-A.

TABLE VIII
RESULTS OF FRW ALGORITHMS FOR FOUR LARGE ITV STRUCTURES

Case	FRW-1				FRW-2				FRW-3					
	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	Sp1*	Sp2*
MIV144	0.542	148K	13.0	3.2	0.542	149K	10.8	2.7	0.542	152K	11.2	1.4	**2.3**	1.9
MIV576	0.544	149K	13.0	11.4	0.544	147K	10.8	9.4	0.543	152K	11.2	1.5	**7.7**	6.4
Viafirst100	3.013	6.3M	36.0	231	3.024	6.2M	13.3	96.0	3.026	6.2M	11.5	35.3	**6.5**	2.7
Viafirst400	3.058	6.1M	36.0	710	3.061	6.1M	13.2	279	3.044	6.2M	11.5	35.0	**20**	8.0

*Sp1 and Sp2 are the speedup ratios to FRW-1 and FRW-2, respectively.

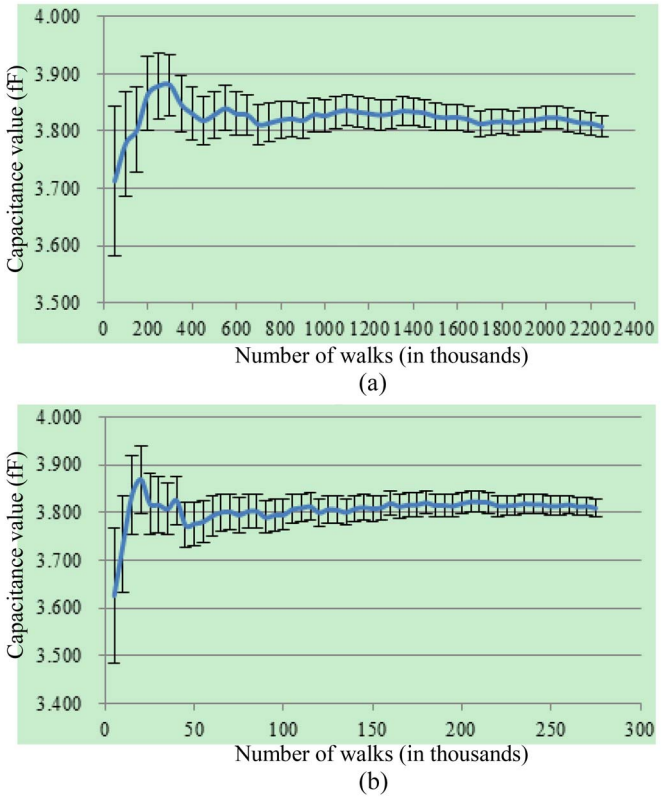

Fig. 15. Convergence behavior of a total capacitance extracted with (a) FRW-3 and (b) FRW-4.

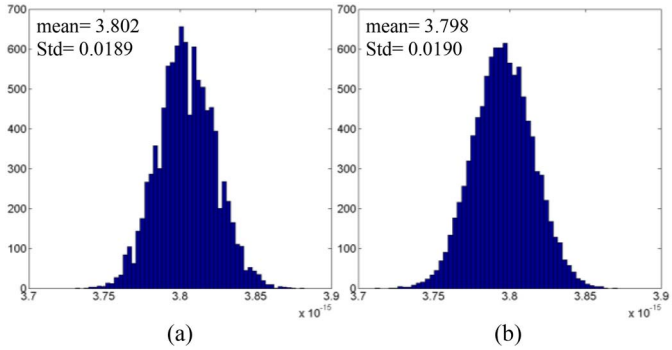

Fig. 16. Distribution of the capacitance extracted with (a) FRW-3 and (b) FRW-4, for 10 000 runs.

"GSP+VR" means the complete FRW-4 algorithm with two techniques. From the table, we see that the GSP version is about 2× faster than FRW-3, which shows the acceleration of FRW convergence due to larger size of the first transition cubes. With the variance reduction technique, the overall speedup ratio of FRW-4 to FRW-3 is up to 12×. The techniques reduce the number of walks largely. And, because the sampling on the Gaussian surface is biased, the average number of hops per walk is also reduced after applying the variance reduction.

In Fig. 15, we compare the convergence behaviors of the total capacitance in the TSV-first case extracted by FRW-3 and FRW-4 algorithms. This figure shows clearly that the optimized importance sampling technique makes the variance decreasing much faster. To completely validate the accuracy of the proposed variance reduction technique, we run FRW-4 for 10 000 times, and then plot the distribution of the extracted capacitance. Fig. 16 shows this distribution for the TSV-first case, accompanied by the distribution obtained with FRW-3. Both plots approximate to the normal distribution, and the calculated Std (≤0.5% of mean value) suggests that the accuracy of capacitance extraction is not degraded with the variance reduction.

The techniques have largely accelerated the FRW-based capacitance extraction for TSV structures. This makes the proposed method is even faster than RWCap handling the square-approximation structures (as already shown in Table II).

D. Results for Multidielectric Cases

We have constructed the multidielectric counterparts for the test cases. The multidielectric cases with TSVs have the dielectric profile like that in Fig. 17(a), while the multidielectric cases with MIVs has the dielectric profile like that in Fig. 17(b). For the TSV cases, the permittivity of thin dielectric layer is 4.2, while the other ILDs permittivity is 3.7. For the MIV cases, the permittivity of thin dielectric layer is 5.0, while the other ILDs permittivity is 2.6. The permittivity of silicon is set to 11.9. Here, TSVs liner is ignored, because it is very thin and can be well modeled with the equivalent dielectric formula in [4]. With the TechGFT program [11], we have built the surface Green's function and weight value tables for the multidielectric structures, which are needed by the FRW algorithms. The results of Raphael, QBEM, and our method are listed in Table X. Due to the memory issue, FastCap broke down for these multidielectric cases. The results of Raphael and QBEM are also not available for some larger cases.

The results in Table X verify the accuracy of our method again. The increase of memory used by the FRW method is due to the multidielectric surface Green's function and weight value tables. The speedup ratio of proposed method to QBEM is up to 143×. Different versions of the FRW algorithms for cylindrical ITVs have also been compared. As the results in Tables VIII and IX for single-dielectric cases, we see similar acceleration of the proposed techniques for the multidielectric cases.

TABLE IX
RESULTS OF FRW ALGORITHMS FOR TSV STRUCTURES

Case	FRW-3				FRW-4									
					GSP				GSP+VR					
	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	C_{tot}(fF)	N_{walk}	N_{hop}	Time(s)	Sp1*	Sp2*
TSV-first	3.811	2294K	11.8	12.7	3.787	950K	15.0	6.4	3.807	280K	11.2	1.66	**7.6**	3.8
TSV-last	3.924	2175K	11.8	12.4	3.915	1568K	14.1	10.1	3.903	458K	11.4	2.79	**4.4**	3.6
TSV-first2	3.782	2324K	11.9	15.1	3.790	956K	15.3	7.5	3.796	282K	11.4	1.90	**7.9**	3.9
Viafirst100	3.100	5741K	11.4	32.1	3.123	1715K	15.2	11.9	3.123	404K	10.9	2.64	**12.2**	5.8
Viafirst400	3.038	5952K	11.5	33.2	3.053	2004K	15.7	14.1	3.034	483K	10.9	3.09	**10.7**	4.5

*Sp1 and Sp2 are the speedup ratios to FRW-3 and GSP, respectively.

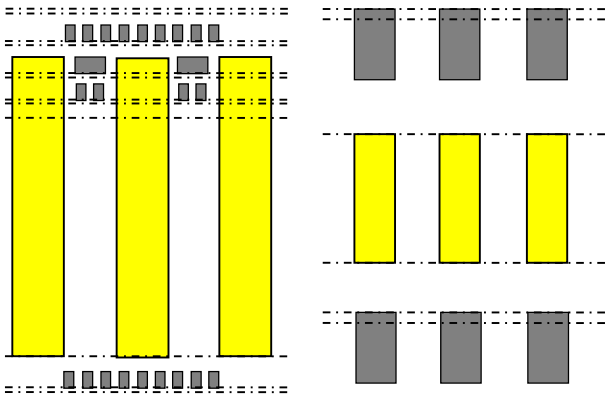

Fig. 17. Cross-sectional view of multidielectric cases. (a) TSV-last. (b) MIV. Short dotted lines stand for dielectric interfaces.

To summarize the numerical results, we have the following remarks.

Remark 1: The square approximation of the cylindrical ITVs brings over 5% error on the total capacitance and much larger error (can be $> 20\%$) on coupling capacitances of ITVs.

Remark 2: The proposed FRW algorithm is able to accurately model the ITV cylinders. Compared with the FRW algorithm only handling square shapes, the proposed method reduces the capacitance error by $10\times$, with no runtime overhead for the TSV structures or some overhead for the MIV structures.

Remark 3: Compared with the simple extension of the original FRW algorithm which still uses the Manhattan transition cubes, the strategy of using rotated transition cubes brings about $2\times$ speedup, while the specific space management, special Gaussian surface placement and importance sampling techniques largely accelerate the computation. Numerical results show that for extracting TSV structures, these techniques contribute from $13\times$ to more than $100\times$ speedup.

Remark 4: BEM-based capacitance solvers are also able to extract the capacitances of cylindrical ITVs. However, their accuracy is not stable, especially on the coupling capacitance. The efficiency of BEM is good for small MIV structures. For TSV or large structures, BEM consumes huge memory and can be several ten times slower than the proposed FRW method.

Remark 5: With different setting of the master conductor, the runtime of FRW-based capacitance extraction may vary a lot. For example, the extraction of a TSV-wire coupling capacitance with a TSV master conductor runs much slower than the extraction of the same capacitance but with a wire set as the master conductor. This is a difference between the FRW algorithm and the BEM for capacitance extraction.

TABLE X
RESULTS OF RAPHAEL, QBEM, AND OUR FRW METHOD FOR THE MULTIDIELECTRIC STRUCTURES (CAPACITANCE IN UNIT OF fF)

Case	Raphael	QBEM			FRW-4				
	Cap.	Cap.	Mem.	Time(s)	Cap.	Err(%)	Mem.	Time(s)	Sp.
TSV-first	33.4	32.56	11GB	534	33.7	0.9	22MB	3.73	**143**
TSV-last	32.9	30.96	5.2GB	188	33.2	0.9	22MB	8.04	**23**
MIV	0.146	0.146	581MB	18.4	0.149	2.1	22MB	2.33	**7.8**
TSV-first2	32.9	31.88	8.8GB	400	33.5	1.8	22MB	7.62	**52**
MIV144	--	0.276	856MB	35.9	0.290	--	23MB	6.33	**5.7**
MIV576	--	0.29	6.7GB	344	0.292	--	25MB	5.69	**60**
Viafirst100	--	--	--	--	26.1	--	28MB	6.37	–
Viafirst400	--	--	--	--	25.3	--	51MB	7.74	–

Remark 6: For the structures with MIVs, the proposed method is about $3\times$ slower than the extraction of the square-approximation structure. It is also slower than the BEM solvers for small MIV structures. Therefore, the application of the proposed method to MIV structures may be restricted to some large-scale cases.

VII. CONCLUSION

To tackle the challenge of accurate parasitic extraction brought by high-density ITVs (TSVs and MIVs) in 3-D ICs, efficient techniques based on the FRW method are proposed to calculate the electrostatic capacitances among cylindrical ITVs and wires. The proposed method is accurate and versatile, and shows advantages over the fast capacitance solvers based on BEM, especially for the structure with TSVs or including a large number of MIVs.

The collaboration of this paper and the ITV model considering semiconductor effect could be explored in the future. The proposed method will be integrated into the RWCap program and shared on the website of the authors.

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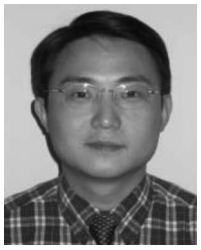

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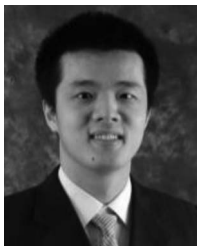

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