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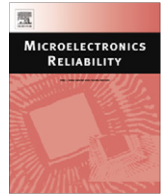

Efficient statistical capacitance extraction of nanometer interconnects considering the on-chip line edge roughness

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ABSTRACT

In this paper, efficient techniques are presented to extract the statistical interconnect capacitance due to random geometric variations, especially the line-edge roughness (LER). Based on the continuous-surface variation (CSV) model depicting wire thickness and width variations, an efficient approach is presented to calculate the capacitance sensitivity with respect to geometric variable, and further the statistical capacitance variance. The Hermite polynomial collocation (HPC) technique with variable reduction is also presented to generate the linear statistical capacitance model. Numerical experiments are carried out on structures in the 45 nm down to the 19 nm technologies. The results demonstrate the presented approaches are several orders of magnitude faster than the MC simulation with 5000 samples. The error of the sensitivity-based approach is less than 10% for the 45 nm structures, while the HPC-based technique exhibits better accuracy, even for the 19 nm structures with strong LER effect.

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1. Introduction

Statistical capacitance extraction is required to capture the uncertainties in the nanometer manufacturing process, and to provide the basis of the effective signal integrity and timing analysis of high-performance integrated circuits. The geometric variation of interconnect wire caused by different mechanisms plays the major role in the statistical capacitance extraction. The thickness variations in metals and interlevel dielectrics (ILD), for instance, are mainly caused by chemical mechanical polishing (CMP), while the lithography steps induce the contour variations. Due to technology scaling, the random variations are becoming prominent. A typical random geometric variation is the line-edge roughness (LER). The LER variation has been extensively studied for the impact on the performance of transistors [1,5], and demands to be considered in the variational capacitance modeling of interconnects [2–4].

Over the past several years, a lot of research has been dedicated to the variational capacitance extraction considering the random variations, whose aim is to derive the statistical metrics of capacitance. The most straight-forward approach is the Monte Carlo (MC) method, where thousands of sample structures are generated and solved with deterministic capacitance extraction algorithm. Therefore, the MC method suffers from the huge computational expense. Several non-MC methods have been proposed, such as the spectral stochastic collocation method (SSCM) in [6], the spectral stochastic method in [7], and the stochastic dominant singular vectors method in [8]. The emphasis of these algorithms is to derive the quadratic variational capacitance model considering the spatially correlated random variables. However, less attention was paid, in these works, to the actual scenario of on-chip process variation, and non-realistic variation parameters were often assumed. In [9], a continuous-surface variation (CSV) model was proposed to describe realistic geometric variations of interconnects, and the Hermite polynomial collocation (HPC) technique is combined with the window-based extraction flow to calculate the statistical full-path capacitance. The CSV model was further improved in [10], and comprehensive analysis and comparison were carried out to reveal its rationality and necessity. This establishes an accurate basis for the statistical capacitance extraction of nanometer interconnects. Notice that most of the above works should be referred to be more theoretical rather than practical, because the demonstrated examples do not match the actual scenario of on-chip variation. Thus, it is a question whether or how the methods can be applied to the current and near-future technologies.

Actually, the magnitude of random variation of on-chip interconnect is not so profound. Therefore, the sensitivities of capacitance are utilized for variational capacitance modeling, which demands much less computational cost. Efficient methods of sensitivity calculation were recently proposed based on the floating random walk method [11] and the boundary element method (BEM) [4,12]. However, in most of these works the nominal

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conductor surface is assumed to vary as a whole. That is, they employ the simplified variation-as-a-whole (VAW) geometric model [10]. This also deviates from actual process technology. In [4], the LER variation was considered in calculating the capacitance sensitivity, but the underlying geometric variation model still has flaw. In [2,3], the variational capacitance caused by the LER was investigated for different technology nodes. However, the model only considers the width variation of interconnect wire, and the expensive MC simulations were employed.

In this paper, we firstly present a comprehensive model to depict the LER and other on-chip random variations. Then, the BEM-based sensitivity approach [4] is extended to collaborate with the CSV geometric model, for extracting the statistical capacitances. Finally, the structures of short-range interconnects in 45 nm down to 19 nm technologies are constructed for performing statistical capacitance extraction. The sensitivity-based approaches and a fast linear-model HPC technique are employed, and are compared with the MC simulation with 5000 samples. The numerical results demonstrate that the CSV-based sensitivity approach is more accurate than the existing technique in [4], and is several thousands times faster than the MC simulation. For the 45 nm technology, the CSV-based sensitivity approach is accurate enough (with error <10%), while its error increases along with the technology scaling, due to the non-equally scaling of LER effect. On the contrary, the linear-model HPC technique achieves less than 8% accuracy for all the technology nodes considered, while its speedup to the MC simulation is several tens to several hundreds. With the both approaches, the statistical capacitance extraction of nanometer interconnects can be performed efficiently. More analysis results and discussion are given in the last sections of this paper.

2. The variation model and existing extraction techniques

In this section, we firstly present the comprehensive model describing the LER and other on-chip geometric variations. Then, the techniques of BEM-based sensitivity calculation and the HPC technique for statistical capacitance modeling are introduced, respectively.

2.1. The model considering LER and other variations

The continuous-surface variation (CSV) geometric model aims to describe the random variations both in thickness and width directions for interconnect wires [10]. Its key point is that the random variables are used to describe directly the fluctuation of discretization vertices, rather than the discretization panels. The latter strategy results in the discontinuous surface variation (DSV) model, as classified in [10]. The variational vertices in CSV model are connected with triangular panels to form continuous surfaces, which reflect the actual physical situation.

In the CSV model, the positive direction of random variation on each surface is the outer normal direction. With only the normal-direction variation, the panel vertices of the both surfaces near an arris would collide with each other, resulting in abnormal variational geometry. To resolve this problem, the derived variable is defined to describe tangential displacement of inner vertex. The value of derived variable is interpolated with the tangential displacement of the surface boundary vertices. In Fig. 1a, the variable setting is illustrated, where ξ^{*}'s denote the derived variables. As an example, the derived variation $\xi^{*}_{y,E}$ at point E is calculated by interpolating the values of y-direction variations $\xi_{y,C}$ and $\xi_{y,D}$. This variable setting preserves the relative spatial relationship of vertices after geometry variation, and thus generates a normal shape with continuous surfaces (see Fig. 1b).

The variational surfaces of an interconnect wire can be classified as top, bottom, left-side, and right-side surfaces. They correspond to

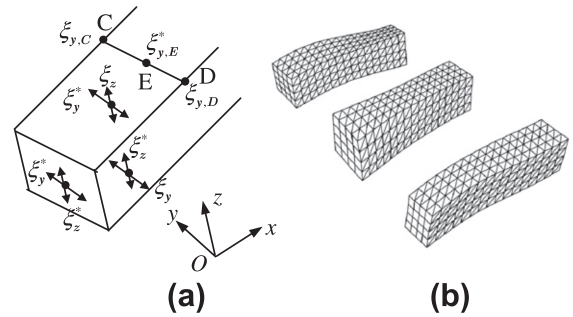

Fig. 1. The illustration of CSV model: (a) surface variable setting and (b) a variational sample of three-parallel-wire structure.

different groups of variables, each of which can be assumed to obey a Gaussian distribution with spatial correlation [10]:

$$\rho(\xi_i) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left(-\frac{\xi_i^2}{2\sigma^2}\right), \tag{1}$$

$$\mathrm{cov}(\xi_i, \xi_j) = \sigma^2 \exp\left(\frac{-|\mathbf{r}_i - \mathbf{r}_j|^2}{\eta^2}\right), \tag{2}$$

where $\rho(\xi_i)$ is the probability density function (PDF) of the i'th variable ξ_i, and σ is the standard derivation (Std). The spatial correlation between two variables are reflected by the correlation function in (2), where η is called correlation length. $\boldsymbol{r}_i$ and $\boldsymbol{r}_j$ are the spatial locations associated with ξ_i and ξ_j, respectively. The larger the correlation length, the stronger the correlation between variables spatially distributed. The ξ's in (1) and (2) can be referred to as the *surface variables*. Because the variations of opposite surfaces are almost independent [2–4,5], the Std of wire width is $\sqrt{2}$ times of the Std of surface variable. So is the Std of wire thickness.

The line-edge roughness (LER) is a typical random variation, arising primarily from polymer aggregation in the photoresist. The LER causes the line-width roughness (LWR). A key metric of LER is the absolute roughness amplitude, equal to 3 σ_{LER} [2–3], where σ_{LER} is the Std of width-direction surface variables in the CSV model. The other key parameter of LER is the correlation length along the line-edge η_{LER} [2–4]. Notice that this parameter only reflects the surface fluctuation along length direction (the x-axis in Fig. 1a), and in the exiting works it is assumed that the LER keeps unchanged along the thickness direction (i.e. the correlation length along z-direction is infinite). To overcome this limitation, we define a z-direction correlation length η_z in this paper. Then, the correlation function for the side-wall variables becomes:

$$\mathrm{cov}(\xi_i, \xi_j) = \sigma^2 \exp\left(-\frac{|r_{i,x} - r_{j,x}|^2}{\eta_{LER}^2} - \frac{|r_{i,z} - r_{j,z}|^2}{\eta_z^2}\right), \tag{3}$$

where $r_{i,x}$ and $r_{i,z}$ stand for the x-coordinate and z-coordinate of the position associated with ξ_i, respectively.

In [2–4], only the side-wall variation (LER) was considered with a DSV-like geometric model. For comprehensive modeling of variations, the wire thickness variation is also included in this work using the CSV model.

There is a significant and worsening gap between current LER in even the highest resolution electron-beam lithography and the LER predicted by the ITRS [1–3]. This means the LER does not scale accordingly and becomes an increasingly larger fraction of wire dimension. Thus, the LER-induced variability is increasingly important for sub-45 nm technologies [3–5,13,15].

2.2. Sensitivity calculation with the adjoint field technique

The adjoint field technique (AFT) was proposed in [12] to calculate the capacitance sensitivity. Using the AFT, the sensitivities can be calculated as a byproduct of capacitance extraction of nominal structure, with little extra expense.

For a system with N conductors, suppose $\boldsymbol{V}$ and $\boldsymbol{Q}$ denote the potentials and charges of conductors, and the matrix $\boldsymbol{C}$ represents the (short-circuit) capacitance matrix. Then,

$$\mathbf{CV} = \mathbf{Q}. \tag{4}$$

Applying Tellegen's theorem to the electrostatic field, we have [12]:

$$(\widehat{V}, (\Delta C)V) = < (\Delta\varepsilon)E, \widehat{E} >, \tag{5}$$

where E is the electric field intensity, and notation "^" indicates the adjoint field quantities. ΔC and $\Delta\varepsilon$ are the effective changes of capacitance matrix and medium permittivity induced by a perturbation of geometric parameter p. Notation "(,)" means the vector inner product, while "<,>" means the inner product of two functions defined by 3-D integral. From (5), it is derived that

$$\widehat{V}^T(\Delta C)V = \int_\Omega (\Delta\varepsilon)E\widehat{E}dr. \tag{6}$$

In order to calculate ΔC_{ij}, the original field is set with $V_j = 1$, $V_k = 0$ $(k \neq j)$, while the adjoint field is set with $\widehat{V}_i = 1$, $\widehat{V}_k = 0, (k{\neq}i)$. Thus,

$$\Delta C_{ij} = \int_\Omega (\Delta\varepsilon)E\widehat{E}dr. \tag{7}$$

Under this setting, the sensitivity of C_{ij} with respect to p is:

$$\frac{\partial C_{ij}}{\partial p} = \lim_{\Delta p \to 0} \frac{1}{\Delta p} \int_{\Omega'} (\Delta\varepsilon)E\widehat{E}dr, \tag{8}$$

while Ω' denotes a local region where the permittivity and electric field change due to the geometry change induced by Δp. In [4,12], where the VAW or DSV geometric model was assumed, Δp is the perturbation of surface panel normal to the surface. Assume Δp causes a set of panels (denoted by S_p) to move from their nominal positions. Thus,

$$\frac{\partial C_{ij}}{\partial p} = -\sum_{k \in S_p} \varepsilon_k A_k E_k \widehat{E}_k, \tag{9}$$

where A_k and E_k are the area and normal electrical field intensity of panel k, respectively. And, ε_k is the dielectric permittivity near panel k. If Δp is very small, the electric field can be regarded unchanged, except for the region where dielectric is replaced by conductor, or vice versa. Thus, Eq. (9) holds.

A special case is that p is only associated with one surface panel (denoted as panel p). It produces the so-called *panel sensitivity* in [4]:

$$\frac{\partial C_{ij}}{\partial p} = -\frac{q_p \hat{q}_p}{\varepsilon A_p}, \tag{10}$$

here q_p and $\hat{q}_p$ are the panel charges in the original and adjoint field settings, respectively.

2.3. The HPC techniques [9]

The variation-aware statistical capacitance $\widehat{C}$ can be expressed with the Hermite polynomial expansion:

$$\widehat{C}(\zeta) = a_0\Psi^0 + \sum_{i_1=1}^{d} a_{i_1}\Psi^1(\zeta_{i_1}) + \sum_{i_1=1}^{d}\sum_{i_2=1}^{i_1} a_{i_1 i_2}\Psi^2(\zeta_{i_1}, \zeta_{i_2}) + \cdots, \tag{11}$$

where $\zeta = (\zeta_1, \ldots, \zeta_d)$ is a set of independent Gaussian random variables, and Ψ^i are the Hermite polynomials of the i'th order. The Hermite polynomial expansion is guaranteed to converge for any Gaussian random process with finite second-order moments. The Hermite polynomials can be labeled consistently to rewrite (11):

$$\widehat{C}(\zeta) = \sum_{j=1}^{\infty} \hat{c}_j \Psi_j(\zeta), \tag{12}$$

where Ψ_j is the j'th Hermite polynomials in ascending order, which satisfy the following orthogonal property:

$$< \Psi_j(\zeta), \Psi_k(\zeta) >_\rho = \alpha_j\delta_{jk}, \quad \alpha_j > 0, \tag{13}$$

where α_j are constant values, and the subscript ρ means that the variables obey the Gaussian distribution. The inner product in (13) is defined as the mathematical expectation of the product of the two stochastic functions:

$$< X, Y >_\rho = E(XY). \tag{14}$$

Eq. (12) can be truncated to get the linear or quadratic approximation of capacitance:

$$C(\zeta) = \sum_{j=1}^{M} c_j \Psi_j(\zeta), \tag{15}$$

where M is the number of Hermite polynomials. The coefficients can be evaluated with:

$$c_j = \frac{1}{\alpha_j} < C(\zeta), \Psi_j(\zeta) >_\rho, \quad j = 1, \ldots, M. \tag{16}$$

According to (14), we need to compute a d-dimensional integral:

$$< C(\zeta), \Psi_j(\zeta) >_\rho = \int C(\zeta)\Psi_j(\zeta)\rho(\zeta)d\zeta. \tag{17}$$

The sparse grid technique can be used to calculate the quadrature in (17), to reduce the computational expense of the conventional Gauss-Hermite quadrature. Thus, (17) becomes an expression of weighted summation:

$$< C(\zeta), \Psi_j(\zeta) >_\rho = \sum_{i=1}^{m} w_i C(\zeta^i)\Psi_j(\zeta^i), \tag{18}$$

where ζ^i is the ith integral point. Therefore, the variational capacitance model can be obtained after solving m deterministic structures defined by the geometric parameters ζ^i. In [9], a weighted principal factor analysis (wPFA) technique is proposed to reduce the random variables in ζ.

3. Two efficient approaches for statistical capacitance extraction

In this section, we firstly combine the AFT and the CSV model to calculate the statistical capacitances of the nanometer interconnects. Then, the techniques for linear-model HPC approach are presented.

3.1. The sensitivity-based approach for the CSV model

In the CSV model, the varying parameter p is associated with vertex, rather than panel. In this case, the formula for capacitance sensitivity (8) is still valid. With the AFT, only the small region where dielectric is replaced by conductor, or vice versa, needs to be considered. In Fig. 2, the discretization of two conductors under the CSV model and the perturbations of geometric variables are shown. We can see that the changed region of a variable p is a kind of pyramid, whose volume is 1/3 of that of prism in [4,12]. So,

$$\frac{\partial C_{ij}}{\partial p} = -\frac{1}{3}\sum_{k \in S_p} \varepsilon_k A_k E_k \widehat{E}_k, \tag{19}$$

where S_p denotes the indices of panels surrounding the disturbed vertex. We further derive:

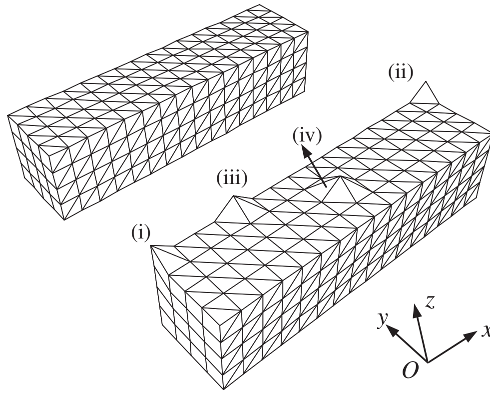

Fig. 2. The perturbation of geometric variables in the CSV model for the sensitivity calculation.

$$\frac{\partial C_{ij}}{\partial p} = -\frac{1}{3\varepsilon}\sum_{k\in S_p}\frac{q_k\hat{q}_k}{A_k}, \tag{20}$$

here we assume that the panels have the same surrounding dielectric with permittivity of ε, which is an usual situation.

Due to the triangular discretization employed by CSV model, the set S_p differs for different location of vertex. As shown in Fig. 2, there are four kinds of situation: (i)–(iv). For them, the sizes of S_p are 2, 1, 3 and 6 respectively.

Once the sensitivity for each variable is obtained, we have the linear-model approximation for a capacitance perturbation ΔC induced by these variables:

$$\Delta C = \sum_{i=1}^{G}\sum_{j=1}^{n_i}\mathcal{S}_{ij}\Delta p_{ij}, \tag{21}$$

where G is the number of variable groups, and Δp_{ij} is the perturbation of the jth variable in the ith group. $\mathcal{S}_{ij}$ denotes the sensitivity, i.e. $\partial C/\partial p_{ij}$. Due to the random nature of variables, the variance and Std of capacitance is needed. The capacitance variance can be calculated based on (21), i.e.

$$\mathrm{var}(C) = \mathrm{var}\left(\sum_{i=1}^{G}\sum_{j=1}^{n_i}\mathcal{S}_{ij}p_{ij}\right) = \sum_{i=1}^{G}\left[\mathcal{S}_i^T\mathrm{cov}(\xi_i)\mathcal{S}_i\right], \tag{22}$$

where ξ_i is the random variables in the ith group, and $\mathrm{cov}(\xi_i)$ is the corresponding covariance matrix. $\mathcal{S}_i$ denotes the column vector of sensitivities: $[\partial C/\partial p_{i1}, \cdots, \partial C/\partial p_{i,n_i}]^T$. And, the Std of capacitance is $\mathrm{Std}(C) = \sqrt{\mathrm{var}(C)}$.

With (20)–(22), the capacitance sensitivities and variances can be calculated for the CSV modeled variational interconnect structure. The sensitivity only depends on panel charges of the nominal structure, and thus can be obtained with once extraction of the nominal structure. The sensitivity-based approach is highly efficient for generating the variational capacitance model for small-magnitude geometric variations. Notice that the sensitivity based approach does not produce the mean value of statistical capacitance, which has little discrepancy to the nominal value if the variation is small enough.

3.2. The linear-model HPC technique

The existing works on HPC or SSCM were mainly focused on obtaining the quadratic model of the variational capacitance [6,8–10]. However, the application of linear capacitance model was almost ignored. Suppose there are d independent random variables, the linear capacitance model is:

$$C(\zeta) = C_0 + \sum_{i=1}^{d}c_i\zeta_i, \tag{23}$$

here C_0 is the mean value of the statistical capacitance, and c_i is the coefficient of Gaussian variable ζ_i. The coefficients C_0 and c_i are calculated with Eq. (16)–(18). Note that (21) and (23) are both linear expressions characterizing the relationship between the capacitance and random variables, but their underlying theory is different. The sensitivity is something about Taylor's expansion, while the linear-model HPC represents an overall fitting of the stochastic function. Therefore, with (23) we may produce capacitance variance with better accuracy than the sensitivity-based approach. Besides, another merit of the HPC technique is that it is able to reveal the difference between the mean value of variational capacitance and the capacitance of nominal structure.

The wPFA technique in [9] is used to reduce the large amount of surface variables to d principal independent variables. Then, with the sparse grid technique, $m = 2d + 1$ integral points are needed to calculate the coefficients in (23). Each integral point corresponds to a set of values of independent variables, and further a variational geometry which can be extracted by a deterministic capacitance solver. Compared with the quadratic-model HPC, which involves $2d^2 + 3d + 1$ integral points, linear-model HPC has much less computational cost but should has enough accuracy for small-magnitude variations. Finally, the parallel computing technique in [10] is also utilized to accelerate the linear-model HPC approach, which can easily achieve more than 85% efficiency of parallelization on a multi-core/multi-CPU platform.

4. Numerical results

In this section, we consider the typical short-range interconnect structures within standard cell, in the 45 nm and below technologies. The sensitivity-based approach and linear-model HPC approach are validated through the comparison with the results of MC simulations. All numerical results are obtained on a Linux server with 8 Xeon CPU cores with 2.13 GHz. The algorithms for statistical capacitance extraction have been implemented in a MATLAB program *statcap*, which invokes FastCap [14] to extract the capacitances for each sample structure. FastCap is a free 3D capacitance solver employing the BEM accelerated by the multi-pole algorithm.

4.1. Settings of numerical experiments

The structure of parallel wires on Metal1 layer is tested, where the LER-induced RC variability is prominent [3]. Fig. 3 shows an example of the test structure. We consider three technology nodes, with interconnect parameters obtained from [13]. The values of wire width, spacing, thickness and dielectric height are listed in Table 1. Because the geometric variation is the major concern, we just assume the single-dielectric situation that the conductors are surrounded by a homogeneous dielectric with relative permittivity of 1.

On the both side-walls of the wires, there is the LER variation. According to [1–3], we assume $3\sigma_{LER} = 6$ nm, and $\eta_{LER} = 20$ nm for all technology nodes. To consider the fluctuation along z-direction,

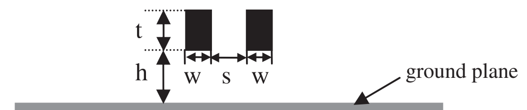

Fig. 3. The cross section of a two-parallel-wire structure.

Table 1
The nominal values of wire width, spacing, thickness and dielectric height in the test cases.

1/2 pitch (nm)	*w* (nm)	*s* (nm)	*t* (nm)	*h* (nm)
45	51	51	92	100
38	43	43	77	85
19	21.5	21.5	43	50

η_z is set to be 1000 nm. For the top and bottom surface variation caused by CMP, we set the Std of top and bottom surface variables to be 1 nm, and the correlation length is 1000 nm. Notice that the actual thickness variation of on-chip interconnects is the superposition of pattern-dependent systematic variation and random variation, and the former is the major factor. Since only the part of random variation is considered in this work, the above setting should be reasonable.

4.2. Results of the sensitivity-based approach

The two-wire structure shown in Fig. 3 is extracted with the CSV-based sensitivity approach, the DSV-based sensitivity approach [4] and the MC simulation with 5000 samples. The computational results are listed in Table 2. Std(C_{11}) is the Std of total capacitance of wire 1, while Std(C_{12}) means the Std of coupling capacitance between wire 1 and 2. Since the sensitivity approach does not produce the statistical mean of capacitance, we list the capacitances of the nominal structure in the table. In this experiment, the length of wires is set to be $L = 100$ nm.

From Table 2, we can see that mean value is very close to the nominal capacitance, whose error is less than 3%. The CSV-based sensitivity method has better accuracy than the DSV-based sensitivity method. This is because that the former approximates the actual situation better. For the 45 nm and 38 nm technology, the CSV-based sensitivity method is able to calculate the Std of total capacitance and coupling capacitance with less than 10% error. However, the error of capacitance Std increases to about 20% for the 19 nm technology. We have varied the length of wires from 50 nm to 500 nm and repeated the experiment. Similar results are obtained, which show the CSV-based sensitivity method produces better accuracy. While for the technology with narrow wires, the sensitivity based approach has larger error due to the prominent LER variation. Notice that, the line-width variation ($3\sigma_{LER} \times 1.414$) under the 19 nm technology has increased to be 39% of the nominal width.

For the two-wire structures, the sensitivity-based method needs to solve the nominal geometry with two settings of bias voltages. While for the MC simulation, 5000 sample geometry are solved. The results in Table 2 show that the speed up ratio of the sensitivity-based method to the MC simulation is about or larger than 3000. The DSV-based sensitivity method is a little bit faster than the CSV-based method, because the former involves fewer surface panels.

Table 3
The computational results for 19 nm-technology two-wire structures (capacitance in unit of 10^{-18} F).

Two wires	Method	Std (C_{11})	Error (%)	Std (C_{12})	Error (%)
$L = 50$ nm	MC-5000	0.180	–	0.147	–
	Sens-CSV	0.151	−**16**	0.122	−**17**
	wHPC-1	0.176	−**2.3**	0.140	−**4.4**
$L = 100$ nm	MC-5000	0.247	–	0.215	–
	Sens-CSV	0.207	−**17**	0.175	−**19**
	wHPC-1	0.234	−**5.5**	0.200	−**7.3**
$L = 200$ nm	MC-5000	0.342	–	0.305	–
	Sens-CSV	0.300	−**12**	0.257	−**16**
	wHPC-1	0.331	−**3.4**	0.293	−**3.9**

Table 4
The computational results for 19 nm-technology three-wire structures (capacitance in unit of 10^{-18} F).

Three wires	Method	Std (C_{11})	Error (%)	Std (C_{12})	Error (%)
$L = 50$ nm	MC-5000	0.240	–	0.147	–
	wHPC-1	0.234	−**2.3**	0.139	−**5.4**
$L = 100$ nm	MC-5000	0.329	–	0.211	–
	wHPC-1	0.325	−**1.3**	0.200	−**5.3**
$L = 200$ nm	MC-5000	0.495	–	0.302	–
	wHPC-1	0.473	−**4.3**	0.291	−**3.6**

4.3. Results of the linear-model HPC approach

As suggested in Section 3.2 that the linear-model HPC would have better accuracy than the sensitivity-based approach, we use it to extract the structures with stronger LER variation. The linear-model HPC employing wPFA (for briefness, we denoted it by wHPC-1) is used to extract the statistical capacitances of the two-wire structure and a similar structure with three parallel wires under the 19 nm technology. The results for cases with different wire lengths are listed in Tables 3 and 4. Since the error of mean value is less than 3% (also demonstrated by other existing works, e.g. [16]), here only the results about the Std of capacitance are listed.

From Table 3, we see that the wHPC-1 is able to reduce at least half error of the CSV-based sensitivity method. The experiments on the three-wire structure produce the similar results. As a whole, the error of wHPC-1 is always less than 8%.

The computational time of wHPC-1 and MC simulation is shown in Table 5. We also list the numbers of independent variables (#variable) and deterministic sample structures for solving (#sample) in the method of wHPC-1. The last row in Table 5 is the time of parallel computing on the 8-core machine, while other data of time are obtained with serial computing. For the purpose of comparison, the #sample for the quadratic-model HPC (wHPC-2) is also given. The quadratic-model HPC has good accuracy [6,9,10], but its

Table 2
The computational results of the CSV-based and DSV-based sensitivity approaches and MC simulation for the two-wire structures (capacitance in unit of 10^{-18} F).

Tech. node	Method	Mean (C_{11})	Std (C_{11})	Error (%)	Mean (C_{12})	Std (C_{12})	Error (%)	Time (s)
45 nm	MC-5000	8.34	0.125	–	−2.97	0.0911	–	8184
	Sens-CSV	8.31[a]	0.117	−**6.2**	−2.95[a]	0.0827	−**9.2**	2.3
	Sens-DSV	8.29[a]	0.111	−**11.3**	−2.94[a]	0.0792	−**13.1**	1.8
38 nm	MC-5000	7.71	0.138	–	−2.85	0.101	–	12,014
	Sens-CSV	7.69[a]	0.127	−**8.2**	−2.83[a]	0.0923	−**8.5**	2.6
	Sens-DSV	7.67[a]	0.121	−**12.7**	−2.82[a]	0.0891	−**11.7**	1.9
19 nm	MC-5000	6.35	0.247	–	−2.90	0.215	–	42,707
	Sens-CSV	6.29[a]	0.207	−**17**	−2.84[a]	0.175	−**19**	7.9
	Sens-DSV	6.27[a]	0.199	−**20**	−2.83[a]	0.170	−**21**	3.0

[a] The capacitance extracted with the nominal structure.

Table 5
The comparison of wHPC-1 and MC method on the computing time.

L (nm)		Two wires 50	100	200	Three wires 50	100	200
wHPC-1	#variable (d)	14	26	42	20	38	62
	#sample (m)	30	54	86	42	78	126
	Time (s)	118	465.7	212.5	217.1	746.4	421.4
wHPC-2	#sample (m)	436	1432	3656	862	3004	7876
MC	Time (s)	20,014	42,707	12,723	26,062	47,956	16,906
Sp. of wHPC-1 to MC		**170**	**92**	**60**	**120**	**64**	**40**
Time of parallel wHPC-1(s)		17.2	70.9	32.7	32.8	112	62.0

computational time is proportional to #sample. So in the experiments, wHPC-2 should be several tens times slower than wHPC-1 and even slower than the MC simulation with 5000 samples. On the contrary, the wHPC-1 is several tens to several hundred times faster than the MC method. While comparing with the sensitivity-based method in Table 2, the paralleled wHPC-1 (time is 70.9s for $L = 100$ nm) is about 10X slower. We think this is the affordable expense for improving accuracy.

5. More analysis results and discussion

Using the both approaches, we can easily analyze the variational capacitance caused by the on-chip random variations. The 45 nm-technology cases in Section 4.2 are the representative of cases with week variation effect, and we tackle them with the CSV-based sensitivity approach. The 19 nm-technology cases are the representative of cases with strong variation effect, which should be extracted with the linear-model HPC technique. The relative standard deviation Std(C)/C is always referred to as "mismatch" by designers, to model the effect of LER and other variation on capacitances. With the 45 nm and 19 nm cases, we can study the relationship between Std(C)/C and the wire length. The simulation results are shown in Figs. 4 and 5, the relative deviation 3Std(C)/C is plotted. On the 8-core machine, the simulation for Fig. 4 only costs 2 min, while the simulation time for Fig. 5 is about 36 min.

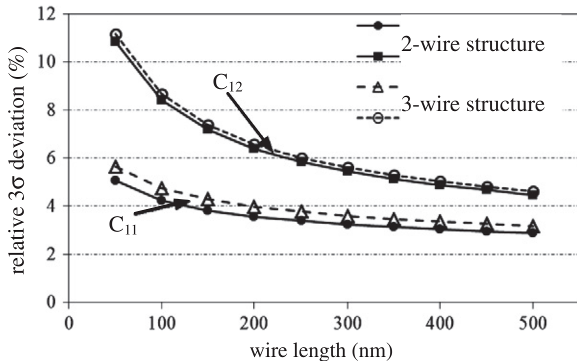

Fig. 4. Plot of capacitance variation as a function of wire length for the 45 nm technology.

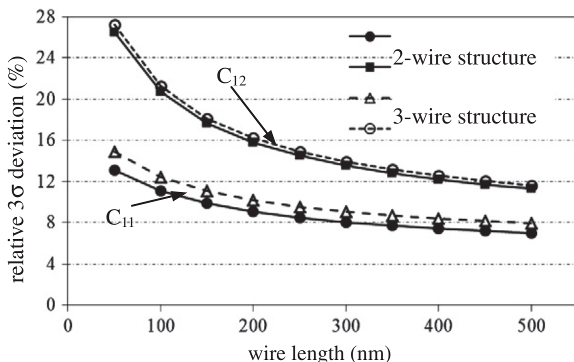

Fig. 5. Plot of capacitance variation as a function of wire length for the 19 nm technology.

From the plots we can see that, as wire length is scaled from 500 nm to 50 nm, the related 3σ deviation increases from about 4% to 11% for C_{12}, under the 45 nm technology. And, there is larger increase of related 3σ deviation for the 19 nm technology (from 12% to 28%). This is because the variation of capacitance is averaged out as the wire length increases. The mismatch of coupling capacitance C_{12} is about double of that of the total capacitance C_{11}. While comparing Figs. 4 and 5, we see that the capacitance variation is doubled if the feature size scales from 45 nm to 19 nm. The capacitance variation is almost inverse proportional to the feature size. Further analysis could be performed, such as to study the impact of parameters σ and η on Std(C)/C. These analysis are useful for circuit designers to estimate mismatches and optimize the critical structures accordingly.

For large structure with longer wire length, the advantage of wPFA accelerated HPC technique will be lost. In that case, the window-based extraction technique [9,16] can be used to reduce the size of structure that the HPC technique handles.

Both the CSV-based sensitivity approach and the linear-model HPC technique are based on utilizing the BEM to solve deterministic interconnect structures. The former uses the surface panel charges extracted from the nominal geometry to generate the capacitance sensitivities (see (20)), while the latter uses the BEM solver to calculate the capacitances (i.e., $C(\zeta^i)$ in (18)) of the sample structures with irregular geometry. So, there is no problem to append the numerical results in this work with the cases with multiple dielectric materials as in reality, since BEM is applicable to multi-dielectric structures [17]. The only difference is that, for multi-dielectric cases, each BEM extraction needs more computational time due to the additional discretization of dielectric interfaces. However, this would not degrade the advantages of the presented techniques for statistical extraction.

6. Conclusions

The main contributions of this work are as follows:

(1) A comprehensive model is established to consider the LER and other random variations of nanometer interconnects, for the 45 nm and below technologies.
(2) The fast BEM-based sensitivity method is extended to consider the accurate CSV model, which improves the accuracy of statistical capacitance extraction.
(3) With the numerical experiments on short-range interconnects with realistic LER effect, we find out that the CSV-based sensitivity approach and a linear-model HPC technique has

sufficient accuracy for extracting the statistical capacitances while exhibiting several orders of magnitude speedup to the MC simulation method. Moreover, the linear-model HPC technique has better accuracy and is applicable for the 19 nm structures with strong LER.

Finally, the presented approaches are very convenient for studying manufacturing variabilities and can be applied to the design optimization for the 45 nm down to 19 nm technologies.

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