The application of boundary element method to the resistance calculation problem in designing flat panel displays

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***Abstract* —** Several techniques are presented for the efficient resistance calculation of wiring structures in flat panel display (FPD). The techniques are based on two-dimensional boundary element method (BEM), suitable for the geometry characteristics of the FPD structures. With an automatic strategy for boundary element partition and the analytical BEM-coupled approach, the proposed resistance solver shows good accuracy and fast computational speed. Numerical experiments demonstrate that the solver can be more than 10,000 times faster than the finite difference solver RAPHAEL while preserving good accuracy. And the proposed techniques accelerate the original BEM remarkably. Structures from real FPD designs have validated the efficiency of the proposed techniques.

Keywords — *boundary element method, computer-aided design, flat panel display, numerical simulation, resistance calculation.*

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1 Introduction

Flat panel display (FPD) has been a widespread and important human-computer interaction device in our daily life. The FPD evolves along two directions. One is very-large-area, high-brightness displays for home television and public information systems. The other is small-area, high-resolution, and low-power displays for mobile devices. In both cases, FPD constitutes one of the key components of cyber-physical system and transforms everyday life for billions of people. The thin-film transistor (TFT)-based active matrix technology is the basis of FPD.[1] According to different lightening mechanism, the FPD employs the liquid crystal display (LCD) technique, or organic light-emitting diodes technique, and so on. There are also different choices for the substrate material, like glass for the normal FPD or plastic for the flexible FPD. Regardless of the techniques and options, designing high-performance and low-cost FPDs is becoming an important topic in electronic design community.[2–7]

Nowadays, the design of high-quality FPD requires specialized computer-aided design tools. A basic design and verification flow of FPD includes steps of schematic design, circuit simulation, pixel design, layout design, layout verification, and mask design (Fig. 1). The panel layout verification includes the design rule check, electrical rule check, and the calculation of parasitic resistance, capacitance, and voltage drop. To validate the signal timing and pursue high-display quality, the resistance and capacitance of interconnect wires in FPD must be considered accurately. This problem is different from the parasitic extraction in designing integrated circuits (ICs). The reason is twofold. Firstly, the proximity of interconnects or between interconnects and the ground in FPD is much less than the proximity of interconnects in IC.[3] Therefore, the parasitic capacitance in FPD is smaller and contributes less to the signal delay than the parasitic resistance. Secondly, instead of pursuing small timing delay in IC design, the most important design metric of FPD is keeping almost equal signal delay to all display pixels. This makes the resistance calculation a crucial task for FPD design. Verifying that the interconnect wires have equal resistance becomes a criterion during the design of high-performance FPDs.

Due to the increase of resolution and the miniaturization trend, the narrow routing area in FPD contains more and more wires connecting the driver circuits and the TFT matrix (Fig. 2). These interconnect wires have complicated geometry, which makes the resistance calculation a challenge. Considering the increasing number of pixels and interconnects in FPD, fast and accurate interconnect resistance calculation becomes a major concern for the success of high-quality FPD products. It should be pointed out that the resistance calculation in FPD is largely different from that in IC design. The interconnect wires in IC are mostly of simple geometry, for example, aligned rectangles. They can be calculated with a simple square-counting approach. For other complex structures, for example, that around the via connecting different metal layers, numerical methods are employed for the resistance calculation.[8,9] Currently, there is no resistance calculation technique specialized for the wiring structures in FPD. Because the signal frequency in FPD wire is relatively low, we mostly care about its DC resistance. Thus, the

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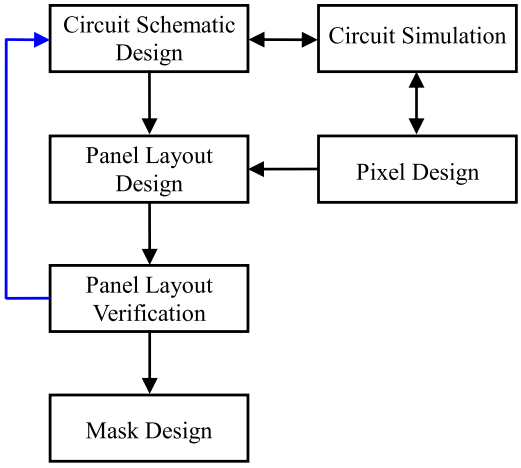

FIGURE 1 — A basic design and verification flow of flat panel display.

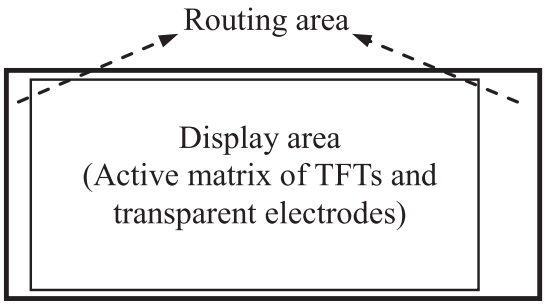

FIGURE 2 — The top view of a narrow-frame flat panel display device. TFT, thin-film transistor.

techniques for extracting the frequency-dependent resistance, like FastHenry,[10] are not suitable for the FPD wires.

The mathematical problem of resistance extraction is solving the Laplace equation in a finite domain. Under preset boundary conditions, it can be resolved with the finite difference method (FDM), finite element method (FEM), or boundary element method (BEM). The first two methods employ domain discretization and generate sparse linear equation system. The last one, BEM, only requires boundary discretization, which produces smaller size but dense linear equation system. For three-dimensional (3D) problem or problems with complex boundary, the BEM often has runtime benefit over FDM and FEM, due to the reduction of dimensionality.[11] BEM has been extensively investigated for the problem of capacitance extraction.[12–15] In the IC design domain, a widely used field solver for resistance and capacitance calculation is RAPHAEL[9] based on FDM. Although with slower computational speed (especially for 3D problem), RAPHAEL is easy to attain the silicon-validated accurate result. This is accomplished by the advanced nonuniform FDM meshing technique in RAPHAEL. So it is usually regarded as the golden standard. The BEM-based methods need more efforts on discretizing the boundaries, and sophisticated techniques for building the linear equation system. Therefore, they are not efficient for 2D problem or the resistance calculation problem with relative simple geometry, as in IC design.

In this work, the resistance calculation problem in FPD design is investigated with specific techniques based on BEM. We have recognized that this is a two-dimensional (2D) problem and developed a resistance solver *Res2d* for FPD interconnect wires. It should be pointed out that there are mainly two kinds of BEM for electrostatic simulation problems. One is indirect BEM,[13,14] and the other is direct BEM.[12,15,16] The former is also called the equivalent charge method and is suitable for infinite-domain problem, while the latter is derived from Green's identity with the free-space Green's function as a weighting function.[11,17] The direct BEM is more suitable for solving a Laplace equation within a finite domain[12] and is therefore adopted in this work. To handle the complexity of FPD wire structures, an automatic boundary element partition and an analytical BEM-coupled approach are proposed. They ensure the computational accuracy and greatly reduce the runtime. Numerical experiments are carried out to demonstrate the suitability of the proposed techniques to the FPD wire structures, and its huge computational speedup.

The remainder of the paper is organized as follows. In Section 2, we explain the mathematical problem of the resistance calculation in FPD design and briefly introduce the direct BEM for resistance calculation. Then, the BEM-based techniques are proposed for the 2D resistance extraction of FPD wire structures. In Sections 4 and 5, the numerical results with actual design structures and the conclusions are given, respectively.

2 Background

In this section, we first describe the resistance extraction problem in FPD design. Then, the direct BEM is briefly introduced.

2.1 The resistance calculation problem in flat panel display

In the process of FPD design, the pixel design (the design of TFT matrix) is separated from the layout design. A major task in the layout design is to route the wires connecting the driver circuits and the TFT matrix. These wires are what we are concerned in this work. In Fig. 3, we show two typical wire structures in FPD. They have unaligned bevel edges, any-angle corners, and may include slits as well. The slits in Fig. 3(a) are used to increase resistance while not weakening the adhesion. The snake-like wire in Fig. 3(b) is also for increasing the resistance within a narrow routing area. The electrical resistance between the two bold edge segments (shown in Fig. 3) is what we want.

Different from the situation in IC design, we shall consider arbitrary 2D geometry for the resistance calculation in FPD. In most cases, 2D simulation is sufficient, because

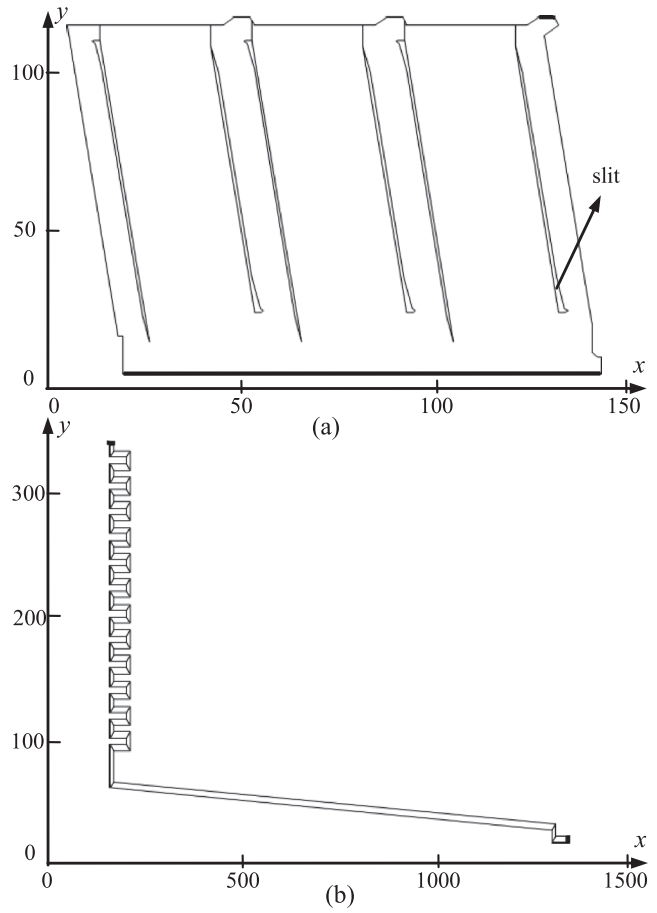

FIGURE 3 — The top view of two flat panel display wire structures: (a) a wire with slits and (b) a snake-like wire. Length unit is 10^{-6} m.

the wires in FPD are usually lied in the same plane and have the same thickness.

To calculate the two-port resistance, the steady-state electric field within the conductor body is simulated. Suppose 1 and 0 V are imposed on the two port edges (denoted by Γ_{u1} and Γ_{u2}), respectively. The resistance equals to the reciprocal of the current flow through Γ_{u1} or Γ_{u2}, that is,

$$R = \frac{V_1 - V_2}{I} = \frac{1}{I} = \left(\int_{\Gamma_{u1}} \sigma \frac{\partial u(\boldsymbol{r})}{\partial \vec{\boldsymbol{n}}} d\boldsymbol{r} \right)^{-1}, \qquad (1)$$

where σ is the conductivity of the wire material, $u(\boldsymbol{r})$ is the electric potential at point $\boldsymbol{r}$, and $\vec{\boldsymbol{n}}$ stands for the normal direction of wire edge. $\partial u(\boldsymbol{r})/\partial \vec{\boldsymbol{n}}$ in 1 is the normal electric field intensity at the port edge. Once the electric field (potential) around the port is solved, with 1, the resistance can be calculated.

The electric potential $u(\boldsymbol{r})$ within the conductor body fulfills the Laplace equation:

$$\nabla^2 u(\boldsymbol{r}) = \frac{\partial^2 u(\boldsymbol{r})}{\partial x^2} + \frac{\partial^2 u(\boldsymbol{r})}{\partial y^2} = 0, \quad \boldsymbol{r} \in \Omega. \qquad (2)$$

Two kinds of boundary conditions are defined as follows:

$$\begin{cases} u(\boldsymbol{r}) = u_0, & \text{at } \Gamma_{u1} \text{ or } \Gamma_{u2} \\ \dfrac{\partial u(\boldsymbol{r})}{\partial \vec{\boldsymbol{n}}} = 0, & \text{at } \Gamma_q \end{cases}, \qquad (3)$$

where Γ_q denotes other boundary (edges) of conductor body except the ports. The second equation in 3 holds because the electric current cannot flow through edge Γ_q. With 2 and 3, the field can be numerically solved with FDM, FEM, or BEM. Then, based on numerical quadrature and 1, the wire resistance is obtained. Note in 2D problem, the resistance result has the unit of Ω·m, meaning the resistance for unit thickness of conductor.

In FPD, it is possible to have a wire with multi-edge port. For example, port 2 may consist of multiple disjoint edges (see Γ_{u2} in Fig. 4). This changes the setting of boundary conditions but brings little difficulty to the numerical methods for resistance calculation.

2.2 Direct boundary element method for two-dimensional resistance calculation

The direct BEM originates from transforming 2 into the following boundary integral equation[11,17]:

$$c_s u_s = \int_\Gamma u_s^*(\boldsymbol{r}) q(\boldsymbol{r}) d\boldsymbol{r} - \int_\Gamma q_s^*(\boldsymbol{r}) u(\boldsymbol{r}) d\boldsymbol{r}, \qquad (4)$$

where u_s is the electric potential at a collocation point $\boldsymbol{s}$, $q(\boldsymbol{r}) = \partial u(\boldsymbol{r})/\partial \vec{\boldsymbol{n}}$ is the normal electric field intensity, and Γ is the boundary of the simulated region Ω. c_s is a constant determined by the boundary geometry around point $\boldsymbol{s}$. $u_s^*(\boldsymbol{r})$ is the fundamental solution of electrostatic field originated from point $\boldsymbol{s}$. For the 2D problem, it has the expression:

$$u_s^*(\boldsymbol{r}) = \frac{1}{2\pi} \ln \frac{1}{|\boldsymbol{r} - \boldsymbol{s}|}, \qquad (5)$$

where $q_s^*(\boldsymbol{r})$ is the derivative of $u_s^*(\boldsymbol{r})$ along the outer normal vector of the boundary.

After discretizing boundary Γ into N constant elements, and setting the collocation points at the center of elements one by one, we get a set of discretized boundary integral equations. They are written as follows:

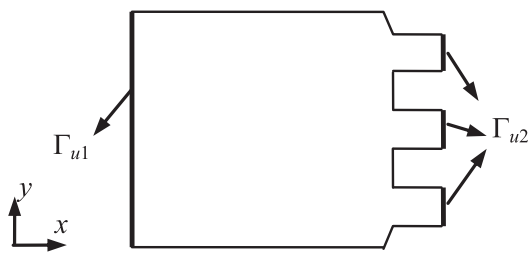

FIGURE 4 — A wire pattern with a multi-edge port.

$$\frac{1}{2}u_k = \sum_{j=1}^{N} q_j \int_{\Gamma_j} u_k^*(\boldsymbol{r})d\boldsymbol{r} - \sum_{j=1}^{N} u_j \int_{\Gamma_j} q_k^*(\boldsymbol{r})d\boldsymbol{r}, \qquad k = 1, \ldots, N, \tag{6}$$

where Γ_j is the j-th boundary element on Γ and u_j and q_j are the potential and normal electric field intensities on Γ_j, respectively. $u_k^*(\boldsymbol{r})$ and $q_k^*(\boldsymbol{r})$ denote the fundamental solution 5 and its normal derivative for the source point at the center of Γ_k, respectively. Note that because we use the constant interpolating function for each 2D element, c_s in 4 all equal to 1/2.

The integrals in 6 can be evaluated with analytical or numerical approach.[15] Then, substituting the boundary conditions 3 into 6, we obtain a linear equation system:

$$\boldsymbol{Ax} = \boldsymbol{b}, \tag{7}$$

where unknown vector $\boldsymbol{x}$ consists of q unknowns in port edges (Γ_{u1} and Γ_{u2}) and u unknowns in boundary Γ_q. $\boldsymbol{A}$ is an $N \times N$ square matrix. After solving 7, with the results of q unknowns on a port boundary and 1, we can calculate the resistance.

Because only the edges of a conductor wire are discretized into elements, the number of unknowns in BEM is much fewer than that in FDM or FEM. Because there is no problem of nonconformal discretization grids like in FDM, BEM will have good accuracy. The drawback of BEM is mainly the dense coefficient matrix of 7. Several fast algorithms have been proposed to sparsify the coefficient matrix or to accelerate the solution of BEM.[12–14] They were mainly used in 3D simulation problems.

3 Direct boundary element method-based techniques for the resistance calculation in flat panel display design

In this section, we present the techniques based on the direct BEM for the resistance calculation of FPD wires. The techniques have been implemented in program *Res2d* and validated with structures from actual FPD design.

3.1 Automatic boundary element partition and equation solution

In BEM, the partition of boundary elements affects both computational speed and accuracy. An automatic boundary element partition approach is important for the ease of applying BEM to engineering problems. A simple strategy of automatic partition can be used for the problem of FPD resistance extraction. We first find the shortest edge on the polygon of conductor wire. With it, we define a basic element size (e.g., one-fourth of the shortest edge's size). Using the basic element size, we can uniformly partition each edge into elements. To make nonuniform partition, we gradually increase the size of basic element for longer edges. Finally, to control the total number of element, we shall set an upper bound for it. If it is exceeded, the element numbers of all edges are scaled down, and then all edges are repartitioned with the adjusted element numbers. An example of boundary element partition is shown in Fig. 5. It should be pointed out that the nonuniform boundary partition involves fewer elements while preserving desirable accuracy.

The quasi-multiple medium approach[12] is able to sparsify the coefficient matrix from the direct BEM by artificially dividing the domain into subdomains. However, it increases the number of unknowns and may also cause the accuracy issue because of the effect of more subdomains on discretization quality. Another algorithm for BEM is the fast multipole algorithm (MPA), which was originally proposed to accelerate the matrix–vector product in indirect BEM.[13] In 1996, Bachtold *et al.*[16] proposed a technique to enhance the MPA to accelerate the direct BEM computation in a finite-domain problem. The MPA is ideal for very large scale problem and may have significant computational overhead for small problem. Therefore, for the 2D problem of FPD resistance extraction, we do not apply the quasi-multiple medium approach or other fast algorithm. This also facilitates implementing an efficient yet robust BEM program.

Because the coefficient matrix of 7 is a dense matrix with a not large order, we employ the method based on LU factorization, or Gaussian elimination, to solve the equation. This can be implemented by ourselves, or by invoking an existing software package. Usually, the latter is a better choice in terms of performance and developing cost. In our *Res2d* program, we use LAPACK,[18] which is the replacer of LINPACK, to solve 7. An optimized basic linear algebra subprograms (BLAS) package called OpenBLAS[19,20] is also employed to achieve better performance. The routines of LAPACK are invoked in our program through the C interface to LAPACK.[21]

3.2 An analytical boundary element method-coupled approach

In FPD, there are some long-wire structures like that shown in Fig. 3(b). If BEM is used to extract their resistances, a large number of boundary elements are involved. This will cause

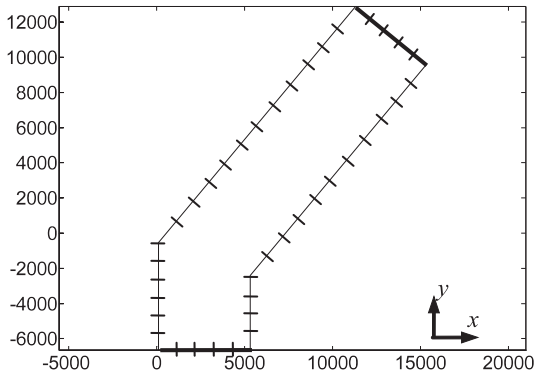

FIGURE 5 — Simple wire structures with any-angle corner.

the computing time greatly increased. After careful observation, we find out that most of these long-wire structures include some portions with rectangle shape. By suitably dividing, the whole resistance can be solved with a divide-and-conquer approach without loss of accuracy.

For the structure shown in Fig. 5, we use RAPHAEL RC2 to simulate its potential distribution under preset port voltages. The equipotential lines are shown in Fig. 6. For this bending wire, the potential around the corner varies disorderly. But at a certain distance from the corner, the equipotential lines become perpendicular to the parallel edges of wire. Therefore, setting a port at this place would not induce error. It separates a rectangle wire from the remained portion of the bend, and the sum of both resistances well approximates the whole wire's resistance. For the rectangle wire, its resistance can be analytically calculated:

$$R_{rec} = \frac{L}{\sigma W}, \tag{8}$$

where L and W are the length and width of the wire, respectively. Note that the thickness (or height) of wire is ignored, as we are considering the 2D resistance. Removing the long-wire rectangles, we can solve the left portions of wire using BEM individually. Because the problem size is largely reduced, the BEM computation usually attains good efficiency. We call this the analytical BEM-coupled approach for the resistance calculation of FPD wires. It is described as the following algorithm.

Algorithm 1: The analytical-BEM coupled approach for FPD resistance calculation 1: R := 0;
2: Calculate the tilt angle θ_i, ($i = 1, \ldots, n$) of all outer-loop edges of the wire profile;

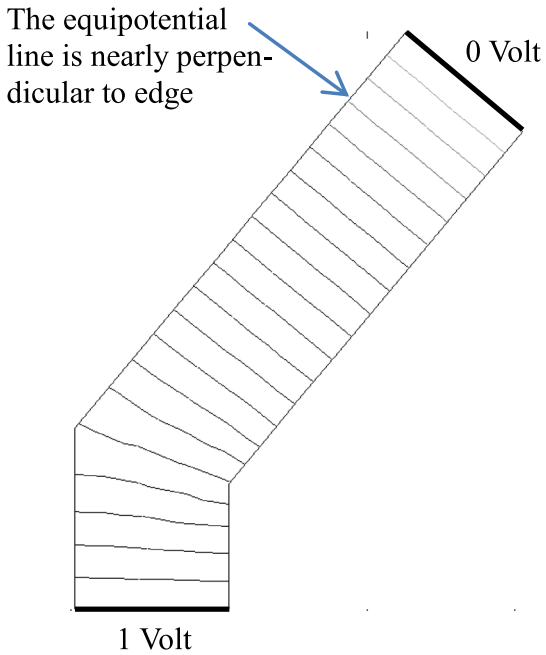

FIGURE 6 — The distribution of equipotential lines on a bending wire.

3: **For** $i = 1,\ldots,n$ //n is the number of outer-loop vertices on the wire
4: **For** $j = i + 1,\ldots,n$
5: **If** $|\theta_i - \theta_i| < \theta_{tol}$, **then**
6: Calculate the valid rectangle;
7: **If** there is a valid rectangle and its length/width ratio > η, **then**
8: Obtain a long-wire rectangle by cutting length of 3X width from the both ends of the valid rectangle;
9: Calculate the resistance R_{rec} of the long-wire rectangle with (8);
10: R:= R + R_{rec};
11: Divide the long-wire rectangle off the wire, and set two ports to the left portions;
12: **Endif**
13: **Endif**
14: **Endfor**
15: **Endfor**
16: **For** each left portion of the wire,
17: Use BEM to calculate resistance R_{lef};
18: R := R + R_{lef}; 19:
EndFor

In Algorithm 1, θ_{tol} is a threshold for determining if the two edges are parallel to each other. η is an aspect ratio, for example, 10. The idea of valid rectangle and dividing from the ends are illustrated by Fig. 7. In Fig. 7(a), the pair of parallel wire edges forms a valid rectangle. By cutting some portions from its ends, we obtain a long-wire rectangle MNPQ. In Fig. 7(b), the perpendicular line does not fall on the edge segment. Therefore, no valid rectangle is formed by the parallel edges AB and CD.

With the analytical BEM-coupled approach, the problem size for BEM computation is largely reduced. More importantly, this hardly affects the accuracy of result. Therefore, with the aforementioned techniques, we are able to develop an efficient resistance solver for FPD wire structures.

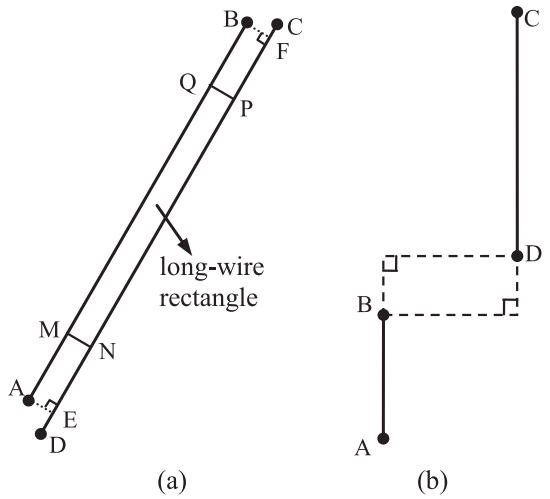

FIGURE 7 — Two parallel wire edges: (a) form a valid rectangle AEFB and (b) do not form a valid rectangle.

4 Numerical experiments

Base on the BEM techniques, we have developed a C language program *Res2d* for calculating the resistance of wire structures in FPD design. *Res2d* invokes LAPACK[18] and OpenBLAS[19] through the LAPACKE interface program,[21] to accelerate the solution of linear equation system. The structures from actual design are tested in the experiments. We first show that the FDM-based RAPHAEL is not suitable or not efficient for the irregular wire geometries in FPD. Then, we validate the efficiency of the proposed techniques. For simplicity, we assume the material conductivity $\sigma = 1\ (\Omega{\cdot}\mu m)^{-1}$ in all experiments.

The experiments are carried out on an Ubuntu Linux server (Linux, Raleigh, NC, USA) with Intel Xeon E5-2630 six-core CPU (Intel, Santa Clara, CA, USA). Unless otherwise stated, the runtime is the CPU time reflecting the efficiency of serial computing.

4.1 The comparison of finite difference method in RAPHAEL and the proposed boundary element method

RAPHAEL is a widely used commercial software for the calculation of resistance and capacitance. It is based on FDM and employs an advanced nonuniform meshing scheme. The RC2 component of RAPHAEL is used to simulate 2D problems. The result of RAPHAEL for capacitance calculation is often regarded as the accuracy criterion by the IC industry. In this subsection, we will show that the RAPHAEL RC2 is inefficient for the resistance calculation in FPD design.

Two structures with any-angle corner and unaligned bevel edges are constructed. They are shown in Figs 5 (Case 1) and 8 (Case 2). The latter is a leaned straight wire that forms an 18° angle with the *x*-axis. In both figures, the bolder lines indicate the ports for resistance calculation. The results of RAPHAEL RC2 under default grid setting and manually set grid numbers are listed in Table 1.

From Table 1, we can see that the resistance value converges with the increase of grid number. At the same time, the computational time increases quickly. For the first case, we assume the result with 10^6 grids is the accurate value. For the second case, the resistance can be analytically obtained which equals to $200\,\Omega{\cdot}\mu m$. So we have the errors of

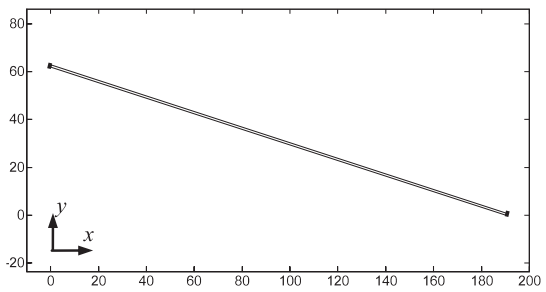

FIGURE 8 — A simple structure with bevel edges (Case 2).

TABLE 1 — The results of RAPHAEL RC2 for extracting the resistance of two simple structures.

Case	Number of grids	Time (s)	R (Ω·μm)	Error (%)
	40,824 (default)	18.58	5.441	31
	100,000	81.25	4.608	11
	500,000	1637.6	4.181	0.7
1	1,000,000	5332.7	4.150	–
	3,472 (default)	1.33	398.2	99
	10,000	6.53	286.2	43
	100,000	104.9	224.8	12
2	1,000,000	3229.9	200.4	0.2

the results under different grid settings. From the table, we see that for both cases, RAPHAEL RC2 cannot produce accurate result unless dense enough discretization grid is imposed. To achieve good accuracy, several thousand seconds of CPU time are needed for this irregular structure of FPD wires.

With the experiment, we reveal that the automatic meshing in RAPHAEL RC2 performs badly for the FPD wire structures. This is totally different from the situation where RAPHAEL is used to handle the regular axis-aligned structures in ICs. Actually, for the structure with bevel edges, the FDM grids are not conformal to the geometry boundary. This may be the reason why it needs very dense discretization to achieve certain accuracy.

For the both cases, the proposed BEM is also used to calculate the resistances, with results listed in Table 2. The error is computed taking the RAPHAEL result in Table 1 as the criterion. From Table 2, we see that the BEM with automatic element partition has good accuracy. To compare the runtime of BEM and RAPHAEL, we consider the RAPHAEL'S results with 5×10^5 grids for Case 1 and 10^6 grids for Case 2. We see that our BEM algorithm is more than 10,000 times faster than RAPHAEL for the two cases. Note that in RAPHAEL, the efficient preconditioned conjugate gradient algorithm with incomplete Cholesky factorization preconditioning is used to solve the sparse linear system.[22] Therefore, the experiment explicitly shows the advantage of BEM over FDM for the 2D resistance calculation problem.

4.2 Validating the LAPACK-based equation solver

In these subsections, five more test cases are simulated to validate the efficiency of the equation solution technique in *Res2d*:

Case A

The example shown in Fig. 3(a).

Case B

TABLE 2 — The results of boundary element method for extracting the resistance of two simple structures.

Case	Number of elements	Time (s)	R (Ω·μm)	Error (%)
1	51	0.014	4.108	1.0
2	208	0.07	199.99	<0.01

The example shown in Fig. 3(b).
Case C
A portion of the example in Fig. 3(b).
Case D
A small case shown in Fig. 9.
Case E
A larger structure similar to that shown in Fig. 3(b).

For comparison, we have also implemented the Gaussian elimination method according to Press.[23] The experimental results are listed in Table 3. For Cases B and E, we cannot get reasonable results from RAPHAEL in tolerable time. These larger cases require a very large FDM discretization grid, which is computationally prohibited. From Table 3, the accuracy of BEM-based techniques is verified again. The times of equation solution reveal that the LAPACK plus OpenBLAS gains speedup for the problem with more than 3000 unknowns. For small problems, it has no advantage because of much time for system calls. Particularly, the LAPACK automatically makes parallel computing on the multi-core CPU. For Cases A and E, the elapsed time (wall-clock time) is 1.68 and 1.92 s, respectively. This means the technique actually brings over 10× speedup to the original Gaussian elimination solver. An automation mechanism has been implemented in *Res2d* to choose the Gaussian elimination method or the LAPACK-based method according to the number of unknowns in BEM computation.

In Table 3, we also listed the runtime of RAPHAEL. From it, we see that our BEM algorithm is at least 329× faster than RAPHAEL for these cases.

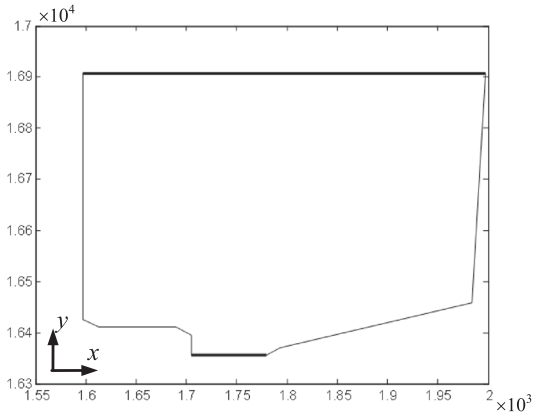

FIGURE 9 — Case D cut from a flat panel display wire. Length unit is 10^{-6} m.

4.3 Validating the analytical boundary element method-coupled approach

We first construct a small case (Case F) to validate the accuracy of the analytical BEM coupling approach. It consists of three connected straight long segments, as shown in Fig. 10. Electrical current flows into the very bottom end and out of the upright end of the wire. The computational results of RAPHAEL under very dense grid and our methods are listed in Table 4. From the table, we can see that coupled approach preserves high accuracy and is several tens times faster than the BEM.

Then, larger cases are tested. One is Case B shown in Fig. 3 (b), and the other is Case G shown in Fig. 11. For each case, the long wire segments are detected, enabling the usage of the analytical BEM-coupled computing method. The computational results are shown in Table 5. From the table, we can see that the coupled approach hardly affects the accuracy (discrepancy <0.5%) while largely reducing the computing time. Due to the large size of the cases, RAPHAEL's result is not available. With careful inspection, we see the resistance of Case G is definitely larger than 9600 Ω·μm, because it involves a long segment with 96,000 μm long and 10 μm wide.

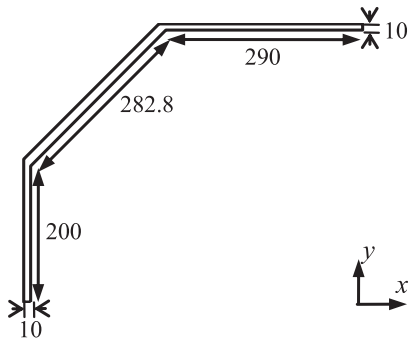

FIGURE 10 — Case F with three long segments. Length unit is 10^{-6} m.

TABLE 4 — The results of *Res2d* with and without the analytical BEM-coupled approach for Case F.

		Number of grids/elements	*R* (Ω·μm)	Time (s)
RAPHAEL RC2		1,000,000	69.83	6338
Res2d	BEM	424	69.74	0.044
Coupled approach	–	69.75	<0.001	

BEM, boundary element method.

TABLE 3 — The computational results of RAPHAEL RC2 and our method for five actual cases.

	RAPHAEL's result			*Res2d*'s result			*Res2d*'s CPU time (s)		
Case	Number of grids (K)	*R* (Ω·μm)	Time (s)	Number of elements	*R* (Ω·μm)	Error (%)	Gaussian	LAPACK	Speedup
A	703	4.158	2513.4	3873	4.183	0.60	24.28	5.54	4.4
B	–	–	–	1547	261.2	–	1.48	2.67	<1
C	100	91.43	82.3	848	90.87	-0.61	0.25	2.13	<1
D	57	2.092	40.1	280	2.08	-0.57	0.01	2.03	<1
E	–	–	–	3931	1770	–	27.8	5.92	4.7

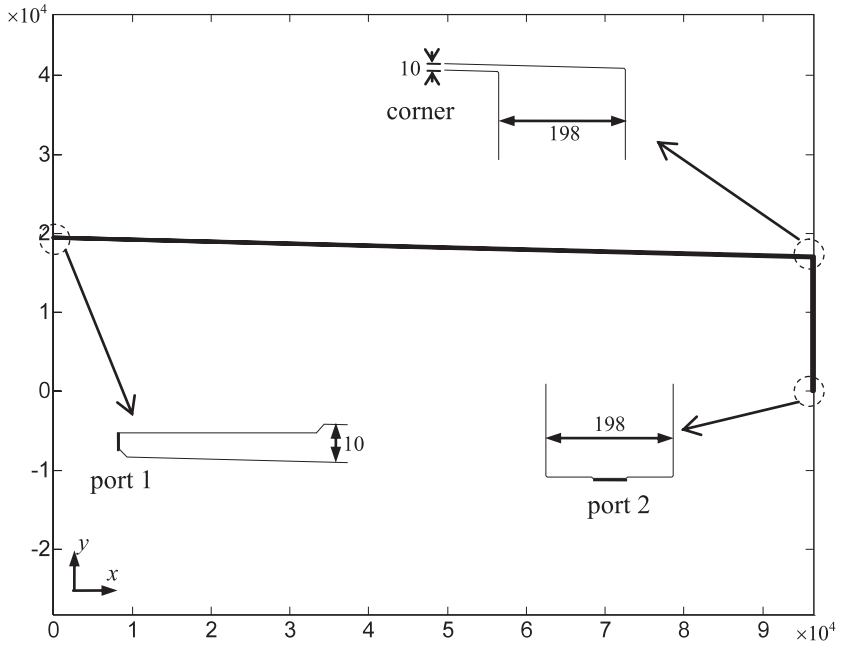

FIGURE 11 — A long flat panel display wire structure (Case G), with zoom-in views of ports and corner. Length unit is 10^{-6} m.

TABLE 5 — The results of *Res2d* with and without the analytical BEM-coupled approach for two large cases.

	BEM			Coupled approach	
Case	Number of elements	R (Ω·μm)	Time (s)	R (Ω·μm)	Time (s)
B	1547	261.2	1.48	261.6	0.92
G	8008	9650	405	9693	0.02

BEM, boundary element method.

This is confirmed by the result obtained from very dense BEM meshing. Note that for Case G, the automatic BEM meshing produces a wrong result of 9154 Ω·μm. Therefore, the analytical BEM-coupled approach provides a necessary supplement for the resistance calculation of FPD wires. Meanwhile, the coupled approach is able to largely accelerate the computation for long-wire structures.

The presented BEM-based techniques have been tested with more than 10,000 wire structures from LCD designs. The results verified the accuracy of the techniques and also demonstrated similar computational speedup as in the presented experiments. Currently, the techniques have been used in a commercial FPD computer-aided design tool,[7] providing crucial support to various FPD design cases. For example, Fig. 12 shows a view of a real layout of smartphone LCD design, where the resistance of the wire outlined in yellow is of interest. From the zoom-in picture, we see that the wire includes both straight segments and slits. The ports are set at the two ends of the wire, indicated by white crosses in Fig. 12. For this case, it costs 15.3 s for the proposed solver to

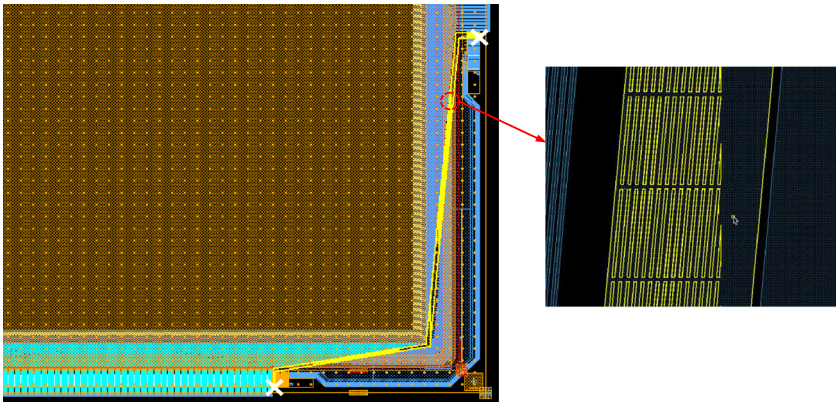

FIGURE 12 — A part of layout of a smartphone liquid crystal display design (the bottom-right corner), where the wire outlined in yellow is the object of resistance calculation. A zoom-in view is given on the right side.

calculate the resistance. The obtained result is 18.138 Ω, which well matches the result from a third-party solver based on FEM. With the proposed solver, it usually costs about 1 h to perform the equal-resistance checking in the layout verification of a smartphone LCD design.

5 Conclusions

In this work, a resistance solver called *Res2d* is presented for the computer-aided design of FPD. The difference between the resistance calculation problems in FPD design and IC design is investigated, which shows the former requires specific treatments and calls for accurate and efficient techniques. To tackle this problem, 2D BEM is applied to extract the resistance per unit thickness of the FPD structure with arbitrary geometry. With an analytical BEM-coupled approach and a simple boundary element partition strategy, the BEM exhibits high accuracy and large acceleration for various FPD structures. Numerical results show that the presented techniques achieve several orders of magnitude speedup without scarifying accuracy. The result of this work is useful for high-quality FPD design and benefits the industrial software. The *Res2d* program has also been shared on the website of the first author.

As the routing space in a FPD is becoming narrower, wires may lie in two metal layers. To calculate the resistance of a wire spanning two layers, we can extend the divide-and-conquer approach used in this paper by separating the metal-layer-to-metal-layer connection region. That region can be simulated with a 3D resistance solver based on BEM,[8] while the left same-metal-layer segments are solved with *Res2d*. Therefore, we can efficiently obtain the total resistance with satisfactory accuracy. This enhancement of our program will be considered in the future.

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