INTERNATIONAL JOURNAL OF NUMERICAL MODELLING: ELECTRONIC NETWORKS, DEVICES AND FIELDS
Int. J. Numer. Model. 2014; **27**:656–668
Published online 26 December 2013 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/jnm.1934

The 2-D boundary element techniques for capacitance extraction of nanometer VLSI interconnects

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SUMMARY

This paper presents several techniques to accelerate the two-dimensional (2-D) direct boundary element method (BEM) for the capacitance extraction of nanometer very large-scale integrated interconnects. Among these techniques, the nonuniform discretization technique minimizes the number of unknowns needed for accurate computation. The technique of adding virtual dielectric interface increases the sparsity of the coefficient matrix. With the technique of blocked Gaussian elimination, the memory usage and CPU time for solving the linear equation system are largely reduced. The analytical primitive functions for the 2-D boundary integrals are also presented. Numerical results show that the presented techniques largely accelerate the 2-D boundary element method. And finally, our BEM-based capacitance solver demonstrates five times speedup over an advanced capacitance solver based on finite difference method. Copyright © 2013 John Wiley & Sons, Ltd.

Received 14 March 2013; Revised 12 May 2013; Accepted 9 August 2013

KEY WORDS: capacitance extraction; boundary element method; nonuniform boundary discretization; analytical integral; virtual dielectric interface

1. INTRODUCTION

With the feature size of integrated circuit (IC) scaling down, the parasitic capacitance of interconnects is making more and more significant impact on circuit performance. In order to carry out detailed simulations emulating actual digital and analog circuit responses, the accurate extraction of parasitic capacitance is a must for building the accurate circuit model for the interconnects in IC. For high-performance circuit design, it is important to make timing verification at the early stage of physical design. This can ensure a faster design closure and reduce the time to market. Hence, after the placement of cells, the static timing analysis is usually performed to find out the signal path violating the timing constraints. This step is very crucial and provides guidelines for the sequent physical synthesis. In [1], a parasitic extraction method is developed for the preroute design stage of very large-scale integrated (VLSI) circuit. This method generates virtual route and estimates congestion by using the placement information of standard cells and then extracting the interconnect parasitics with the pattern-library method. In this scenario, two-dimensional (2-D) geometric patterns depicting the cross sections of interconnect structures are used for the capacitance extraction. The capacitances of patterns are calculated in advance with the field solver algorithms and stored in a table or as interpolation formulas. Therefore, the preroute parasitic extraction can be performed very quickly and with sufficient accuracy for the design optimization.

The field solver methods for calculating the capacitance mainly include domain discretization method and boundary integral equation method. The domain discretization methods are the finite difference method (FDM) and the finite element method (FEM) [2]. The boundary integral equation

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methods are also called boundary element method (BEM). The FDM and FEM discretize the entire domain, producing a sparse linear equation system with larger order. They are more mature and possibly more efficient than BEM, especially for 2-D cases. Several widely used commercial capacitance solvers, such as Raphael^{TM} of Synopsys and Q3D^{TM} of Ansoft, are based on FDM or FEM.

The BEM is a numerical method for solving linear partial differential equations that are formulated as integral equations (i.e., in boundary integral form). It can be applied in many areas of engineering and science including fluid mechanics, acoustics, electromagnetics, and fracture mechanics [3–5]. BEM has also been applied to electromagnetics [6–10], such as the capacitance extraction problem, where it is also called the method of moments [6]. In BEM, only the boundaries are discretized; hence, a much smaller system of linear equations is obtained. Also, problems encountered with complex boundaries can be effectively handled with BEM, whose accuracy is generally considered to be superior to that of FDM and FEM. Thus, the BEM with rapid computing techniques has become the focus of research on field solvers for capacitance extraction.

In the practice of applying BEM to capacitance extraction problem, the most time-consuming part is the generation and solution of the linear equation system. Although the linear equation of BEM is relatively small when comparing with volume discretization counterparts, it is usually dense. There have been several algorithms proposed to accelerate the matrix–vector products and further the solution of BEM equations. Among them, the most famous one is the fast multipole method (FMM), which applies multipole and local expansions to approximate the effect of remote panels on the evaluation panel [9]. However, this FMM-based methodology is suitable for large-scale examples. In the problem of establishing the capacitance library of 2-D patterns, all patterns are small and regular. Therefore, the FMM is not the best choice, because of its computation overhead [8].

In this paper, we propose the techniques for developing an efficient BEM-based 2-D capacitance solver for VLSI interconnects. First, we propose a nonuniform approach to discretize the conductor surface according to the analysis of the electric field distribution. This technique reduces the number of boundary panels without loss of accuracy. Then, the analytical results of the 2-D boundary integrals are deduced. It expedites the generation of the linear equation system as compared with using the numerical integral technique [11]. Finally, a virtual dielectric interface is added to the 2-D interconnect pattern structure. This increases the sparsity of generated linear equation system. Together with the blocked Gauss equation solving technique, the solving time of BEM equations is largely reduced. The proposed techniques are integrated into a solver call BECap2D. It has replaced the Raphael rc2 solver used in [1] for building the pattern library for the preroute parasitic extraction. Numerical experiments are carried out on the 2-D interconnect patterns under a typical 45-nm process technology. Our BEM solver is able to accurately model the features in the nanometer process technology and has shown five times speedup over the advanced capacitance solver Raphael.

The remainder of this paper is organized as follows. Section 2 outlines the direct BEM [10, 11] and related techniques for calculating the interconnect capacitance. The proposed techniques for 2-D capacitance extraction are presented in Section 3. The numerical results are presented in Section 4. Finally, we draw conclusions in Section 5.

2. THE DIRECT BEM FOR INTERCONNECT CAPACITANCE EXTRACTION

2.1. Fundamental formulation of BEM

With m conductor embedded in M dielectrics layers, the relation between the potentials of m conductors, denoted by $V \in \mathbb{R}^m$, and the charges on each conductor, denoted by $Q \in \mathbb{R}^m$, is given by $Q = CV$, where $C \in \mathbb{R}^{m \times m}$ is referred to as the capacitance matrix. To obtain the jth column of the capacitance matrix, the potential of the jth conductor is set to be 1 V, and the potential of the rest conductors is set to be 0 V. The jth conductor is called the master conductor, and the rest conductors are called environment conductors.

DOI: 10.1002/jnm

Within the domain of the ith dielectric denoted by Ω_i, the electrical potential u is governed by the Laplace equation with mixed boundary conditions:

$$\begin{cases} \nabla^2 u = \dfrac{\partial^2 u}{\partial x^2} + \dfrac{\partial^2 u}{\partial y^2} = 0, \text{in } \Omega_i \; i = 1, \ldots, M \\ u = u_0, \text{on } \Gamma_u \\ q = \dfrac{\partial u}{\partial \boldsymbol{n}} = 0, \text{on } \Gamma_n \end{cases}, \tag{1}$$

where Γ_u is the Dirichlet boundary (surface of conductors), with u known and determined by preset bias voltage; Γ_n is the Neumann boundary (outer boundary of simulated domain), where the normal electrical field intensity q is supposed to be zero. $\boldsymbol{n}$ stands for the unit vector outward normal to the boundary. Besides, u and q fulfill the compatibility equations along the interface of two adjacent dielectrics a and b as follows:

$$\begin{cases} \varepsilon_a \dfrac{\partial u_a}{\partial n_a} = -\varepsilon_b \dfrac{\partial u_b}{\partial n_b}, \\ u_a = u_b \end{cases} \tag{2}$$

where ε_a and ε_b stand for the permittivities of dielectric a and b.

With the direct BEM, the electrostatic Laplace equation is transformed into the following direct boundary integral equation (BIE) [3, 7]:

$$\frac{1}{2} u_s + \int_{\partial\Omega_i} q^* u d\Gamma = \int_{\partial\Omega_i} u^* q d\Gamma, \tag{3}$$

where u_s is the electric potential at point s on boundary. u^* is the fundamental solution of Laplace equation. For 2-D case, u^* is $(1/2\pi)\ln(1/r)$, where r is the distance between the source point and field point. q^* is the derivative of u^* along the outer normal vector of the boundary. $\partial\Omega_i$ is the boundary surrounding the homogenous dielectric subregion i.

After discretizing boundary Ω_i into N_i constant elements, the discretized form of the direct boundary integral equation can be written as follows:

$$\frac{1}{2} u_k + \sum_{j=1}^{N_i} u_j \int_{\Gamma_j} q_k^* d\Gamma = \sum_{j=1}^{N_i} q_j \int_{\Gamma_j} u_k^* d\Gamma, \qquad k = 1, \ldots, N_i, \tag{4}$$

where Γ_j is the jth boundary element on $\partial\Omega_i$, and u_j and q_j are the potential and normal electric field intensity on Γ_j, respectively.

2.2. Setup of the linear equation system

The integrals in (4) can be classified as singular and nonsingular integrals. When the source point lies in the interval to be integrated, that is, $k = j$ in (4), it is the singular integral. Brebbia [11] gives the analytical results for the singular integrals:

$$\begin{cases} \int_{\Gamma_i} u_i^* d\Gamma = 0.5 \\ \int_{\Gamma_i} q_i^* d\Gamma = \dfrac{1}{\pi} \times r_1 \times \left[\log\left(\dfrac{1}{r_1}\right) + 1 \right] \end{cases}, \tag{5}$$

where r_1 is the half length of the integral interval.

If $k \neq j$ in (4), it becomes the nonsingular integral. Usually, numerical methods, such as the Gauss–Legendre formula, are employed to calculate the nonsingular integrations [11]. The numerical method is straightforward and easy to be implemented. However, it has larger computational expense, especially for the nearly singular integration, where a considerably high order of numerical integration is needed for a reasonable accuracy.

DOI: 10.1002/jnm

After reorganizing the equation systems (4) to make all unknown variables collected in a left-hand side vector, and the known values of u and q in the corresponding right-hand side, we can write the result linear equation as the standard form as

$$\boldsymbol{Ax} = \boldsymbol{b}, \tag{6}$$

where the coefficient matrix $\boldsymbol{A}$ is large and nonsymmetric. For the organization of discretized BEM equations (4), an approach has been proposed in [13]. According to it, all the unknowns in the discretized BIEs can be classified into three types: v_{ii}, u_{ij} $(i<j)$, and q_{ij} $(i>j)$, where the subscript stands for the dielectrics the unknown belongs to. Then, source points and unknowns are properly arranged so that the nonzero blocks in the coefficient matrix $\boldsymbol{A}$ are greatly reduced. As to an interconnect structure with stratified dielectrics shown in Figure 1, the order of unknowns is v_{00}, u_{01}, q_{10}, v_{11}, u_{12}, q_{21}, …, $u_{n-2,\ n-1}$, $q_{n-1,\ n-2}$, $v_{n-1,\ n-1}$. So, the nonzero coefficients are regularly located in the diagonal blocks and several blocks adjacent to the main diagonal (Figure 2).

2.3. Blocked Gauss equation solving technique

With the schemes introduced in Section 2.2 to properly arrange the unknowns, the linear matrix $\boldsymbol{A}$ is a sparse blocked coefficient matrix for multidielectric problem. In [3], a blocked equation solving technique is presented. We briefly introduce it as follows and apply it to the capacitance extraction. Consider a 2×2 blocked equation system:

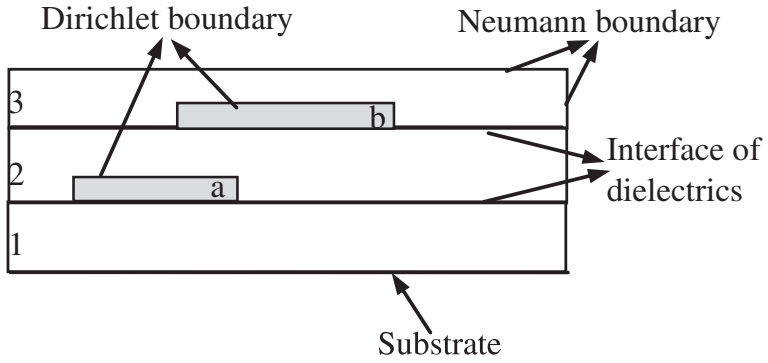

Figure 1. A typical capacitor with three stratified dielectric layers.

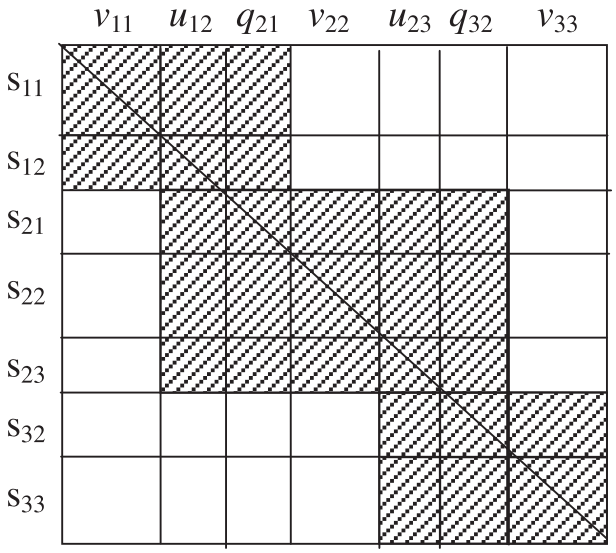

Figure 2. The coefficient matrix population for the case in Figure 1.

DOI: 10.1002/jnm

$$\begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} b_1 \\ b_2 \end{pmatrix}. \tag{7}$$

The dimensions of entries $\boldsymbol{A}_{11}$, $\boldsymbol{A}_{12}$, $\boldsymbol{A}_{21}$, $\boldsymbol{A}_{22}$, $\boldsymbol{b}_1$, $\boldsymbol{b}_2$, $\boldsymbol{x}_1$, and $\boldsymbol{x}_2$ are $n\times n$, $n\times m$, $m\times n$, $1\times n$, $1\times m$, $1\times n$, and $1\times m$, respectively. This equation can also be expressed as follows:

$$\begin{cases} A_{11}x_1 + A_{12}x_2 = b_1 \\ A_{21}x_1 + A_{22}x_2 = b_2 \end{cases}. \tag{8}$$

Left multiply (8) by A_{11}^{-1} to symbolically solve for $\boldsymbol{x}_0$ as follows:

$$x_1 = A_{11}^{-1}b_1 - A_{11}^{-1}A_{12}x_2. \tag{9}$$

Substituting (9) into (8) then yields the following:

$$\left(A_{22} - A_{21}A_{11}^{-1}A_{12}\right)x_2 = b_2 - A_{21}A_{11}^{-1}b_1. \tag{10}$$

Solve (10) for $\boldsymbol{x}_2$ and then substitute $\boldsymbol{x}_2$ into (9), the $\boldsymbol{x}_1$ is obtained. This idea is the same as the common Gauss elimination except that the entries are submatrices. Note that A_{11}^{-1} in this procedure is purely symbolic, that is, the matrix inverse need never be computed explicitly. In (10), the coefficient matrix $\left(A_{22} - A_{21}A_{11}^{-1}A_{12}\right)$ can be regarded as the updated diagonal block $\boldsymbol{A}_{22}$. The right-hand side vector $\left(b_2 - A_{21}A_{11}^{-1}b_1\right)$ can be regarded as the updated $\boldsymbol{b}_2$ in the same way. This 'updating' idea allows us to generalize this process to treat the $N\times \underline{N}$ blocked matrix provided all diagonal blocks are square.

In blocked sparse matrices, nondiagonal block may be a zero matrix. In (9), for example, if $\boldsymbol{A}_{12}$ is known to be a zero block, there is no need to compute $A_{11}^{-1}A_{12}x_2$. Therefore, this equation solving technique will greatly reduce the computation effort for a blocked sparse equation, such as that generated in BEM-based capacitance extraction. The algorithm of block Gauss equation solution is described as Algorithm 1.

Algorithm1: Block Gauss equation solving technique

```
//step 1: blocked LU factorization
For(i=1; i<N; i++)
{
      LU(Aii);
      For(j=i+1; j<N; j++)
      {
            Aii·D=Aij ;                  //solve D, D=inv(Aii) · Aij
            for(k=i+1;k<N;k++)
                  Akj:= Akj - Aki·D ;
      }
}
LU(Aii);
//step 2: block forward-reduction
For(i=1; i<N; i++)
{
      Aii·Ci=bi ;                        //solve Ci, Ci=inv(Aii) · bi
      for(j=i+1; j<N; j++)
            bj:= bj - Aji· Ci;
}
//step 3: block back-substitution
For(i=N; i>=1; i--)
{
      Aii·Xi=bi;                   //solve Xi, Xi=inv(Aii) · bi
      for(j=i-1; j>=0; j--)
            bj:= bj - Aji· Xi;
}
```


DOI: 10.1002/jnm

This algorithm shows good adoption to equation systems generated from discretized BIEs in the following three aspects:

1) All diagonal blocks are square: As introduced in the beginning of this section, the equation organization makes source points and field points the same in the diagonal blocks of the matrix. This guarantees that all diagonal blocks are square, which accords with the requirements of blocked Gauss method.
2) No addition of nonzero entries: The most difficult problem in blocked Gauss method is that zero entries may become nonzero in LU factorization phase (the 'fill-in' phenomenon). However, it can be avoided for stratified dielectric structures.
3) No need to choose the primary entry: With consistency of source points and unknowns, singularity of the integral kernels makes diagonal entry of the matrix with large absolute value. For this reason, the computational result is accurate enough without choosing primary.

About the memory usage, there is almost no additional assumption except for the memory to store the original sparse blocked coefficient matrix, because the LU factorization for diagonal blocks can be carried out in the original matrix and the interim matrix $D = A_{ii}^{-1}A_{ij}$ can be computed column by column. So, exactly speaking, the additional memory space for the whole solution phase is only an $n \times 1$ vector, where n stands for the size of the largest diagonal block. This is negligible compared with the additional space requirement of the Krylov subspace iterative equation solvers.

3. ACCELERATING TECHNIQUES FOR THE 2-D CAPACITANCE EXTRACTION WITH BEM

3.1. Nonuniform boundary discretization

The boundary discretization scheme largely affects the number of unknowns in the linear equation system. The naive way for the boundary discretization is to divide all boundaries into intervals with equal length. However, usually a large number of unknowns are needed for a reasonable accuracy if no optimizing approach is adopted. It is intuitive that different boundary elements have different impacts on the accuracy of final result. On the one hand, the fundamental solution of Laplace equation, that is, $u^* = (1/2\pi)\ln(1/r)$, is inversely proportional to the distance between the source point and the evaluation point. As we are evaluating the capacitance of master conductor, the boundaries that are far away from the master conductor has less impact on the final result. Hence, it is natural to discretize those boundaries coarsely while discretizing other boundaries finely. On the other hand, with the shielding effect of electrostatic field, the boundaries that are shielded away from the master conductor by environmental conductors have negligible impact on the capacitance of the master conductor. Hence, the discretization of them can be quite coarse without loss of accuracy.

In [12], the capacitance coupling between conductors is classified into different types in order to derive the analytical approximating formulas for the capacitances. Specifically, the coupling capacitance is considered to have the components of plate capacitance, terminal capacitance, and fringe capacitance (Figure 3). Inspired by Zhao *et al.* [12], we classify the boundary similarly and make

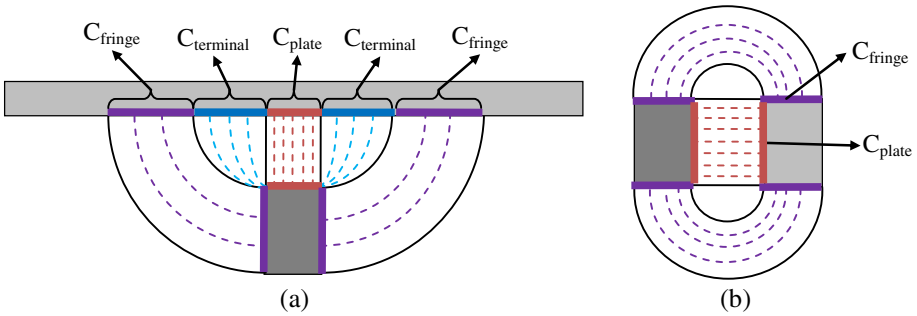

Figure 3. The illustration of electrical field between (a) master conductor and long line, (b) master conductor and side conductor.

DOI: 10.1002/jnm

nonuniform discretization. We first recognize regions that are induced by different types of coupling effects, that is, plate region, terminal region, fringe region, and the remaining region. Then, we discretize them with different granularities. The approach to recognize the regions is illustrated in Figure 4, where Figure 4(a) illustrates the region denoted as plate regions. In the plate regions, the electrical fields between the master conductor and environment conductors are the strongest. As a result, the related boundary is discretized denser. Figure 4(b) illustrates the terminal regions whose electrical fields are induced by the corner of master conductor. The discretization density of the boundaries within the terminal regions is just second to the plate regions. Figure 4(c) illustrates the fringe region whose electrical fields induce fringe capacitance. The electrical field of fringe region is weaker. So, the discretization in it is coarser than the previous two as well. In case that more than one region overlapped in a same area, the highest discrete density of the overlapped regions is adopted. The boundaries that have not been recognized by the previous regions have the lowest discretization density. On the basis of our numerous experiments, we found that when the discretization densities of those four types of regions have a ratio of 5:3:2:1, the result has the best balance between performance and accuracy.

3.2. Analytical boundary integrals

In this subsection, we deduce the analytical results for the 2-D boundary integrals. By comparing the results of analytical formulas with the results of numerical integration, we can see the remarkable promotion in the speed and accuracy.

Figure 5 illustrates the integrals we want to calculate. When the source point, say $p_s(x_s, y_s)$, does not lie in the integral interval, the integral is a nonsingular one. Otherwise, the result can be obtained with (5). We denote the two endpoints of the integral interval as $p_1(x_1, y_1)$ and $p_2(x_2, y_2)$. Assume the integral direction is from p_1 to p_2. We use t_1 as a parameter to present every point on the integral interval:

$$\begin{cases} x(t_1) = x_1 + t_1(x_2 - x_1) \\ y(t_1) = y_1 + t_1(y_2 - y_1) \end{cases}. \tag{11}$$

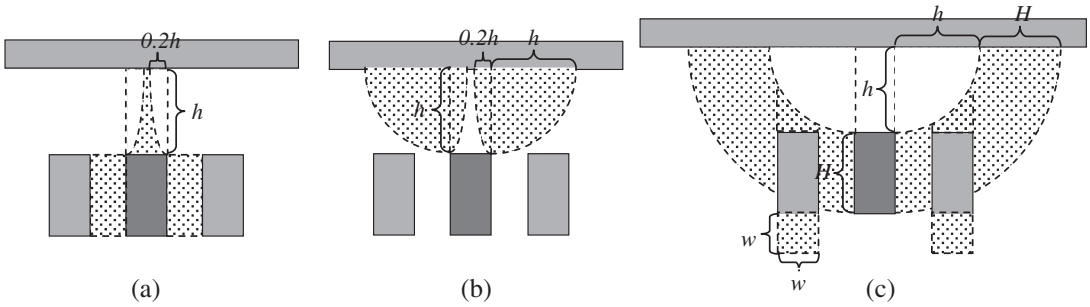

Figure 4. The classification of regions based on the relative position with master conductor. The red block stands for the master conductor, the brown blocks stand for environment conductors, the shadowed blocks stands for the regions (a) plate region, (b) terminal region, (c) fringe region.

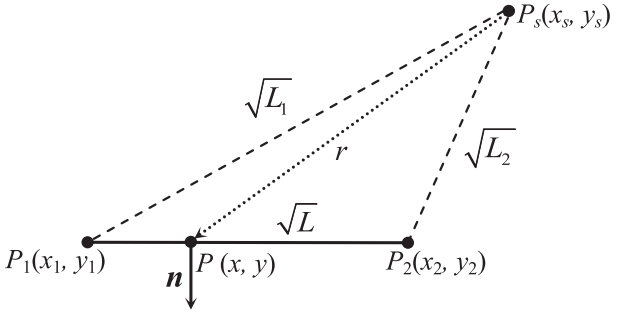

Figure 5. Illustration of the integral, where P_s is the source point, P_1 and P_2 are two terminals of the integral interval, $\boldsymbol{n}$ is the unit out normal vector.

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The distance from $p_s(x_s, y_s)$ to a point $p(x(t_1), y(t_1))$ on the integral interval, denoted by $r(t_1)$, can be written as

$$r(t_1) = \sqrt{(x_1 + t_1(x_2 - x_1) - x_s)^2 + (y_1 + t_1(y_2 - y_1) - y_s)^2}. \tag{12}$$

The primitive function of the potential-integral kernel function can be obtained by the following:

$$\begin{aligned} \int u^* d\Gamma &= \int \frac{1}{2\pi} \ln\left(\frac{1}{r(t_1)}\right) d\Gamma = \int \frac{1}{2\pi} \ln\left(\frac{1}{r(t_1)}\right) \sqrt{(x'(t_1))^2 + (y'(t_1))^2} dt_1 = -\frac{L}{2\pi} \int \ln r(t_1) dt_1 \\ &= -\frac{L}{4\pi} \begin{cases} 2t \ln(t_1) + \ln(L) - 2 & , \quad \text{when } \Delta \le 0 \\ \frac{1}{L}\sqrt{\theta}(x_1 - x_0) \tan\left(\frac{2t_1 L}{\sqrt{\theta}}\right) + t_1 \ln\left(t_1^2 + \frac{\theta}{2L}\right) + \ln(L) - 2, & \text{otherwise} \end{cases} \end{aligned} \tag{13}$$

where L is square of the length of the integral interval, that is, $L = (x_1 - x_2)^2 + (y_1 - y_2)^2$. L_1 and L_2 are the squares of the distance from p_1 and p_2 to p_s, respectively, that is, $L_1 = (x_s - x_1)^2 + (y_s - y_1)^2$, $L_2 = (x_s - x_2)^2 + (y_s - y_2)^2$. The values of θ and Δ are

$$\begin{cases} \theta = 2LL_1 + 2LL_2 + 2L_1L_2 - L^2 - L_1^2 - L_2^2 \\ \Delta = 4L^2L_1^2 - \left(L_2^2 - L_1^2 - L^2\right)^2 \end{cases}. \tag{14}$$

The normal electrical field intensity q^* is numerically equivalent to derivative of potential along the unit out normal vector:

$$q^* = \frac{\partial u^*}{\partial \boldsymbol{n}} = \nabla\left(\frac{1}{2\pi} \ln\left(\frac{1}{r}\right)\right) \cdot \boldsymbol{n} = -\frac{1}{2\pi r^2} ((x - x_s, y - y_s) \cdot \boldsymbol{n}), \tag{15}$$

where $\boldsymbol{n}$ is the unit out normal vector at the point of (x, y), as shown in Figure 5. Because all boundary elements are lines, the unit out normal vectors of every point on a same boundary panel is the same, we have

$$\boldsymbol{n} = \frac{1}{\sqrt{L}} (y_2 - y_1, x_1 - x_2). \tag{16}$$

To calculate the primitive function of the integral, we first transform the second kind integral into first kind integrals, and this gives

$$\begin{cases} H_x(t_2) = \dfrac{(x_2 - x_1) \ln\left(Lt_2^2 + 2(L_2 - L_1 - L)t_2 + L_1\right) + 2(y_2 - y_1) \arctan\left(\dfrac{Lt_2 + L_2 - L_1 - L}{(x_1 - x_0)(y_2 - y_1) - (y_1 - y_0)(x_2 - x_1)}\right)}{2L} \\ H_y(t_2) = \dfrac{(y_2 - y_1) \ln\left(Lt_2^2 + 2(L_2 - L_1 - L)t_2 + L_1\right) + 2(x_2 - x_1) \arctan\left(\dfrac{Lt_2 + L_2 - L_1 - L}{(x_1 - x_0)(y_2 - y_1) - (y_1 - y_0)(x_2 - x_1)}\right)}{2L} \end{cases}, \tag{17}$$

where t_2 is the substituted integral variable. The lower and upper limits of t_2 are 0 and 1, respectively. The dot product of the first kind integrals with the norm out vector is exactly the value of the original second kind integral, that is, the integral of the norm out field density:

$$\int q^* d\Gamma = \int \frac{\partial u^*}{\partial \boldsymbol{n}} d\Gamma = \frac{1}{L} \left(H_x(t_2), H_y(t_2)\right) \cdot (y_2 - y_1, x_1 - x_2). \tag{18}$$

With formulas (13) and (18), we can obtain the nonsingular integral value to avoid the using of numerical integral.

DOI: 10.1002/jnm

3.3. Virtual dielectric interface

As mentioned before, BEM often leads to dense matrixes. The cost of the establishing and solving of the matrixes are proportional to the number of nonzero elements in the matrixes. During our experiment, we observed that after our nonuniform discretization strategy, most nonzero elements of the linear equation concentrate in the layer where the master conductor is located. Another important observation of BEM is that the elements in a same dielectric domain compose a nonzero block in the linear equation, and elements from different dielectrics have interactions only when they are on the same boundary. Therefore, we propose to add a virtual dielectric interface at the position of the bottom of the master conductor to reduce the nonzero entries of the linear equation. In Figure 6, we show a cross section structure of VLSI interconnects and the corresponding BEM coefficient matrices before and after adding the virtual dielectric interface.

From Figure 6, we see that before adding virtual dielectric interface, the elements in the layer where the master conductor is located compose a large nonzero block. After adding the virtual dielectric interface, the original domain is divided into five subdomains (A–E in Figure 6(b)). Although a slightly more boundary elements is introduced on the newly added interface, the new linear is much sparser than the original. With the adopting of the blocked linear equation solving technique introduced in Section 2.3, whose computation cost is proportional to the number of nonzero elements in the linear equation, the solving speed can be accelerated, as shown in Section 4. Another merit of this technique is that it is very easy to be implemented. The only extra work is to find the bottom position of the master conductor and add a new interface there, which is almost negligible.

4. NUMERICAL RESULTS

Our experiments are based on a typical 45-nm process technology, which contains eight metal layers [14]. The parameters of each metal layer are listed in Table 1. Under the nanometer technology, the side edges of conductors are not vertical but with an oblique angle of α. The oblique angle of the side edge is described by its tangent value. In our experiment, it is set that $\tan\alpha = 0.1$. The cross section view of the 45-nm technology is shown in Figure 7.

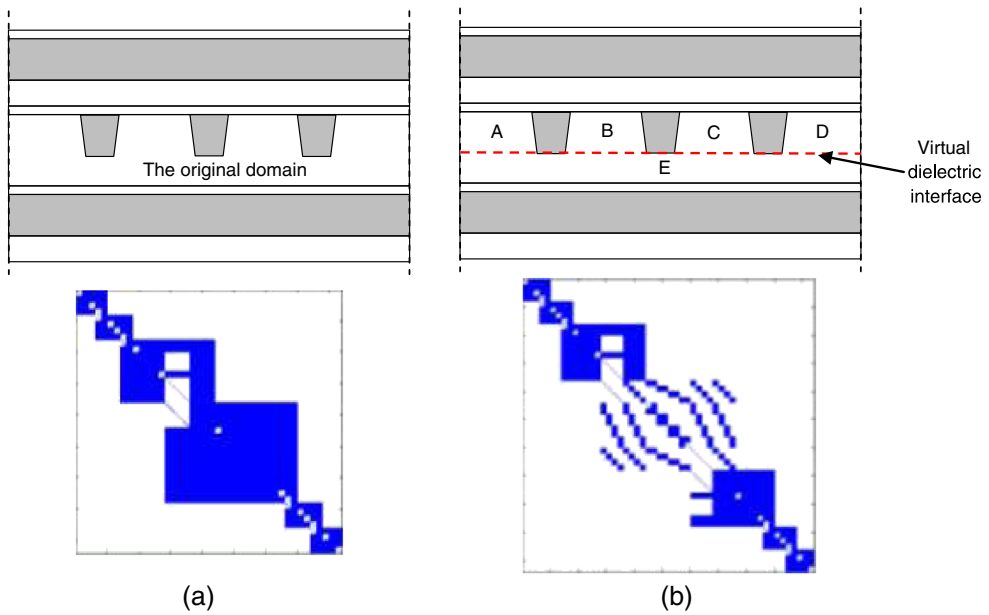

Figure 6. The illustration of the virtual dielectric interface adding technique. (a) The cross-section view of the structure and its corresponding linear equation before introducing the virtual dielectric interface. (b) The cross-section view of the structure and its corresponding linear equation after the introducing of the virtual dielectric interface.

DOI: 10.1002/jnm

Table I. The parameters of each metal layer for a typical 45-nm technology.

Layer	Minimum wire width (nm)	Wire thickness (nm)	Minimum wire space (nm)
POLY	45	58	45
Metal 1	70	140	70
Metal 2	70	140	70
Metal 3	70	140	70
Metal 4	100	180	100
Metal 5	120	200	120
Metal 6	140	220	140
Metal 7	160	240	160
Metal 8	180	270	180

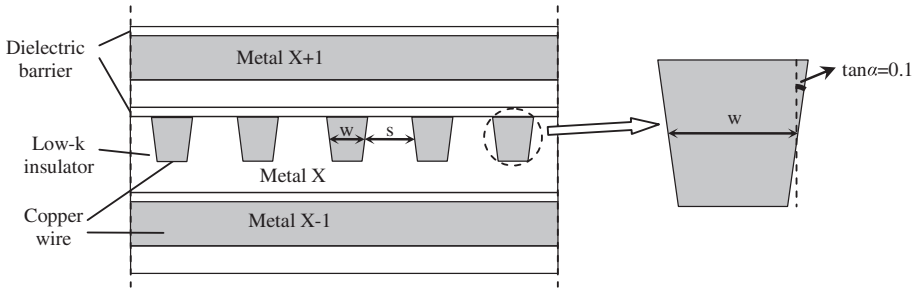

Figure 7. The cross section view of a 45nm technology a technology with dielectric barriers.

For the multilayered interconnects in VLSI circuit, some experiments were carried out in [15] to reveal the major capacitance effects. Several useful conclusions are as follows.

1) For the wires in the same layer with the master conductor, only the coupling capacitances of the nearest neighbor wires are needed to be considered, for example, wires C_a and C_b in Figure 8. The capacitances of other wires are negligible.
2) In order to reduce the crosstalk between adjacent metal layers, the wiring directions of adjacent layer wires are always perpendicular. Therefore, on the cross section view along the wiring direction of the master conductor, there might be parallel lines on the adjacent layers. The corresponding place might also be vacant if the corresponding place happened to be the space between wiring. When the corresponding place is vacant in the adjacent layer, the location on the further layer can be treated as a parallel line with neglectable error, because of the densely routing nature of ICs.

With the aforementioned conclusions, we established the interconnect patterns for capacitance library. In each pattern, the master conductor is located at the center of the simulation region, with two environment conductors at the same layer on its left and right sides, respectively. There are two metal blocks located in the upper and lower metal layers of the master conductor, respectively. The

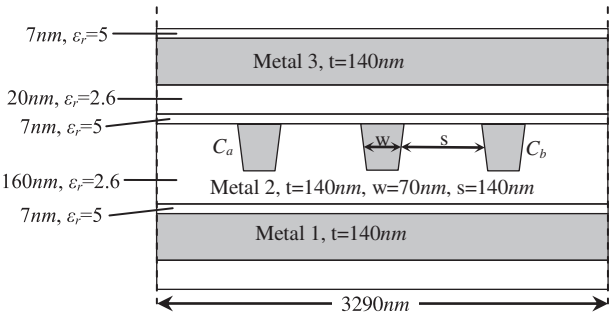

Figure 8. The illustration of the model with the master conductor in the layer of Metal 2.

DOI: 10.1002/jnm

wire width of the master conductor is the multiply of minimum wire width, from 1 time to 6 times. The wire space between the master conductor and the environment in the same layer is the multiply of minimum wire space, from 1 time to 6 times. Figure 8 gives an example pattern when the master conductor is in the layer of metal 2, the wire width is the minimum wire width, that is, $w = 70$ nm, and the wire space is twice the minimum wire space, that is, $s = 140$ nm. The pattern library is the combination of patterns with all possible parameter settings. We have a total of $C_9^3 \times 6 \times 6 = 3024$ patterns for the typical 45-nm technology with eight metal layers.

To evaluate the efficiency of the used blocked Gauss solving technique, we compared it with other equation solving techniques. For a case from the aforementioned patterns, the times for solving the linear equation systems are listed in Table 2. The proposed analytical boundary integrals are used, because it does not affect the equation solution. The '\' operator in MATLAB is the state-of-the-art direct sparse solver, which employs the UMF-PACK algorithm for general sparse matrix [17]. And, the iterative generalized minimal residual (GMRES) method for the nonsymmetric matrix is also tested [18]. The Jacobi and ILU preconditioners are applied to the GMRES algorithm, respectively.

As shown in Table 2, the blocked Gauss technique demonstrates the best performance. In general, iterative solvers are effective for large and highly sparse equations. For our cases, the matrix dimension is not large, and the sparsity is not high, for example, 82% for approach (C) with virtual interface for increasing the sparsity. So, the performance of iterative solvers is not as good as direct solvers. The MATLAB '\' operator is also slower than our approach, because it does not exploit the particular block structure in the coefficient matrix. It can also be indicated from Table 2 that after the introduction of virtual dielectric interface, the time for solving the equation increases a little because of the increase of unknowns. However, the time for generating the matrix is reduced because fewer integrals are needed to calculate the nonzero entries.

With the proposed techniques, we have developed a BEM solver called BECap2d in C language. With it and Raphael rc2 [16], all patterns described earlier are simulated to extract the capacitances. Note that Raphael rc2 is a widely used commercial finite difference solver using the techniques of advanced nonuniform meshing and the incomplete Cholesky decomposition preconditioned conjugate gradient iterative equation solver. The result of Raphael is regarded as the golden value for capacitance extraction. The experiments are run on a Sun Fire V880 server with a frequency of 750 MHz. The computational time of different approaches are listed in Table 3.

Regarding the results of Raphael rc2 as the criterion, we also give the average capacitance errors with different BEM techniques in Table 3. From the table, we see that with the proposed techniques, the accuracy of BECap2d is comparable with that of Raphael. Note that for the simulated structures with oblique boundaries, the FDM needs the interpolation to match the discretization grid to the boundary. On the contrary, the BEM has no difficulty to handle the complex geometry. Therefore, it is generally acknowledged that BEM is more accurate than FDM for the problems with complex geometries. From Table 3, we also see that the original BEM without accelerating technique is slower than Raphael, despite that the number of unknowns in the former is fewer than that in the latter. And, the larger error of original BEM is mainly due to the inadequate boundary element partition. With the nonuniform discretization approach in Section 3.1, the number of unknowns in BEM is largely reduced, while the computational accuracy is largely improved. Although adding the virtual dielectric interface introduces

Table II. The performance of several linear equation solvers for a case from our patterns.

Approach no.	Method description	No. of unknowns	No. of nonzero entries	Matrix generating time (ms)	Matrix solving time (ms)			
					Blocked Gauss	MATLAB '\'	GMRES (Jacobi)	GMRES (ILU)
(A)	BEM + analytical integral	840	20,4560	105.1	**37.3**	56.2	222.6	652.7
(B)	(A) + nonuniform discretization	214	12,014	10.0	**1.1**	3.2	9.4	13.5
(C)	(B) + virtual interface	240	10,192	8.8	**1.2**	5.0	12.2	11.4

DOI: 10.1002/jnm

Table III. The total CPU time for extracting the 3024 patterns with different approaches.

Approach no.	Extracting method	Average no. of unknowns	Total time (s)	Average error versus Raphael (%)
(A)	Raphael rc2	2506	2170	—
(B)	Original BEM	827	2972	15
(C)	(B) + nonuniform discretization	232	1431	2.6
(D)	(C) + virtual interface	255	1002	3.1
(E)	(D) + analytical integral	255	431	2.8

extra unknowns, the sparsity of linear equation system is increased. From Table 3, we see that this technique averagely improves the computational speed up to 42%. The adoption of the analytical integral formulas largely accelerates the setup of linear equation system. With all the accelerating techniques, BECap2d becomes five times faster than Raphael while preserving good accuracy.

5. CONCLUSIONS

In this paper, several techniques are proposed to accelerate BEM for the capacitance extraction of nanometer VLSI interconnects. The nonuniform boundary discretization technique is proposed on the basis of the analysis of electric field distribution, which largely reduces the number of unknowns needed for accurate computation. The analytical formulas are deduced to replace the numerical integration of 2-D boundary integrals. It accelerates the generation of discretized BEM equations. Finally, by adding a virtual dielectric interface, we largely improve the sparsity of the overall coefficient matrix. With a block Gauss equation solver, the time for solving the linear equation system is further reduced. Numerical experiments are carried out on the interconnect patterns for the 45-nm process technology, with trapezoidal cross section and multiple dielectric layers. Compared with the advanced FDM solver, the accelerated BEM solver exhibits five times advantage on computing time, while preserving good accuracy.

ACKNOWLEDGEMENT

The authors acknowledge the financial support from the National Natural Science Foundation of China under Contract No. 61076034, and the Beijing Natural Science Foundation under Contract No. 4132047.

REFERENCES

1. Gong W, Yu W, Lü Y, Tang Q, Zhou Q, Cai Y. A parasitic extraction method of VLSI interconnects for pre-route timing analysis. *Proc. International Conference on Communications, Circuits and Systems* (*ICCCAS*), 2010; 871–875.
2. Sumant P, Cangellaris A. Algebraic multigrid Laplace solver for the extraction of capacitances of conductors in multi-layer dielectrics. *Int J Numer Model* 2007; **20**:253–269.
3. Kane JH. Boundary Element Analysis in Engineering Continuum Mechanics. Prentice Hall: New Jersey, 1994.
4. Tao Y, Shen ZX, Zheng BY. Analysis of quadruple corner-cut ridged square waveguide by hybrid mode-matching boundary-element method. *Int J Numer Model* 2011; **24**(1):24–35.
5. Milsom RF, Scott KJ. Radio frequency simulation of a complex printed circuit board layout by the quasistatic boundary element method. *Int J Numer Model* 1988; **1**(3):165–170.
6. Mehta DP, Chakrabarty SB. Moment method analysis for capacitance and charge distribution of dielectric coated metallic disk and closed truncated cone isolated in free space. *Int J Numer Model* 2013; **26** (2):127–139.
7. Yu W, Wang Z, Gu J. Fast capacitance extraction of actual 3-D VLSI interconnects using quasi-multiple medium accelerated BEM. *IEEE Trans Microwave Theory Tech* 2003; **51**(1):109–119.
8. Hsiao YC, El-Moselhy T, Daniel L. Efficient capacitance solver for 3D interconnect based on template-instantiated basis functions. *Electrical Performance of Electronic Packaging and Systems* (*EPEPS*), 2009; 179–182.
9. Nabors K, White J. FastCap: a multipole accerlerated 3-D capacitance extraction program. *IEEE Trans Computer-Aided Design* 1991; **10**(11):1447–1459.
10. Yu W, Wang Z, Hong X. Preconditioned multi-zone boundary element analysis for fast 3D electric simulation. *Eng Anal Bound Elem* 2004; **28**:1035–1044.
11. Brebbia CA. The Boundary Element Method for Engineers. Pentech Press: London, 1978.
12. Zhao W, Kang SH, Cao Y. Field-based capacitance modeling for sub-65-nm on chip interconnect. *IEEE Trans Electron Devices* 2009; **56**(9):1862–1872.
13. Yu W, Wang Z. Organizing and storing of discretized BEM equations in 3-D multi-dielectric parasitic capacitance extraction. *Proc. 4th International Conference on ASIC*, Shanghai, China. 2001; 677–680.
14. Deschacht D, Rivaz S, Farcy A, Lacrevaz T, Flechet B. Keep on shrinking interconnect size: is it still the best solution? *Proc. IEMT*, 2010; 1–4.
15. Cong J, He L, Kahng AB, Noice D, Shirali N, Yen SC. Analysics and

justification of a simple, practical 2 1/2-D capacitance extraction methodology. *In Proc. of the 34th annual Design Automation Conference, DAC*, 1997; 627–632.

16. Synopsys Inc.. Raphael: 2D, 3D resistance, capacitance and inductance extraction tool. http://www.synopsys.com/Tools/TCAD/InterconnectSimulation/Pages/Raphael.aspx
17. UMFPACK version 5.6. http://www.cise.ufl.edu/research/sparse/umfpack.
18. Saad Y. Iterative Methods for Sparse Linear Systems (2nd). SIAM Press: Philadelphia, 2003.

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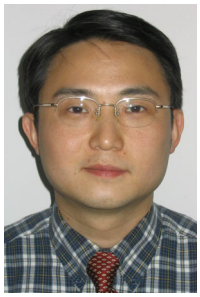

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DOI: 10.1002/jnm