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PAPER

Efficient Partial Reluctance Extraction for Large-Scale Regular Power Grid Structures

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SUMMARY Inductive effect becomes important for on-chip global interconnects, like the power/ground (P/G) grid. Because of the locality property of partial reluctance, the inverse of partial inductance, the window-based partial reluctance extraction has been applied for large-scale interconnect structures. In this paper, an efficient method of partial reluctance extraction is proposed for large-scale regular P/G grid structures. With a block reuse technique, the proposed method makes full use of the structural regularity of the P/G grid. Numerical results demonstrate the proposed method is able to efficiently handle a P/G grid with up to one hundred thousands wire segments. It is several tens times faster than the window-based method, while generating accurate frequency-dependent partial reluctance and resistance.

key words: *high-frequency effect, inductance modeling, parasitic extraction, partial reluctance, power/ground grid*

1. Introduction

As VLSI circuit integrates more than a thousand million transistors with working frequency of multiple giga-hertz (GHz), the circuit's power consumption increases exponentially. This calls for low-power design techniques, and increases the request of performing accurate and complete full-chip analysis to guarantee power integrity. Therefore, accurate modeling and dynamic simulation of the power/ground (P/G) grid is becoming critical for VLSI circuit design and verification.

Modeling the inductive effect of on-chip and off-chip interconnects is another research focus for current nano-scale VLSI chips. The conventional RC model of interconnect is not sufficient for accurate circuit analysis. Moreover, the reduction of resistance by copper and capacitance by low-k dielectric highlights the inductive effect; the denser geometries and growing complexity of interconnect structures bring challenges to on-chip inductance modeling and extraction [1].

One major difficulty to capture the inductance effect is the unknown return path prior to extraction and circuit simulation. This problem was solved by the partial element equivalent circuit (PEEC) model, where the partial inductance defined with the return path at infinity was adopted [2]. However, the resulting inductance matrix is dense due to the coupling of partial inductance among all conductors. This prevents it from being applied to large-scale interconnect structures, such as the P/G grid.

In the partial inductance matrix, faraway coupling entries may be small, but simply truncating them would make the system unstable [3]. To overcome the inefficiency brought by the dense partial inductance matrix, a concept of partial reluctance (or, K-element) was proposed in [4]. The partial reluctance matrix $\boldsymbol{K}$ is the inverse of partial inductance matrix, i.e.

$$\boldsymbol{K} = \boldsymbol{L}^{-1}, \tag{1}$$

where $\boldsymbol{L}$ is the partial inductance matrix. The partial reluctance has a locality property similar to capacitance, so that circuit simulation based on it is much more efficient than that based on partial inductance [4]. Later papers [5]–[8] showed the circuit simulation was greatly accelerated by using the partial reluctance. It was proved that, with small matrix entries ignored, the sparsified partial reluctance matrix is positive definite and the subsequent circuit simulation is stable [5]. Now, the partial reluctance has been supported by industrial circuit simulators, like HSPICE [9].

The inductive effect of on-chip P/G wires is becoming inevitable. Furthermore, the high-frequency effect, i.e. the skin effect and proximity effect, should be considered for some wider P/G wires. Several methods of partial reluctance extraction have been proposed to consider the high-frequency effect. In [10], an algorithm was presented to extract the frequency-dependent partial reluctance. The algorithm is actually an extension of the double-inversion idea proposed in [8]. Wei et al. [11] borrowed the locality of partial reluctance for admittance at ultra high frequency and obtained an extraction algorithm for frequency- dependent inductance and resistance. A direct extraction approach, combined with the window technique was proposed in [12], which avoids the double-inversion computation [8], [10] and demonstrates higher efficiency for frequency-dependent partial reluctance extraction. The algorithm was then improved in equation solving [13] and reinforced through calculating frequency-dependent resistance [14].

The on-chip P/G grid may involve thousands of wire segments. Such a large size presents a significant challenge to accurate modeling and simulation of the P/G grid. Shi et al. [15] proposed a pattern idea to accelerate the DC simulation of the P/G grid, which explores the geometry character-

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istics of regular P/G grid and translates topology similarity to sub-matrix regularity. They divided the whole P/G grid into blocks on the X-Y plane, and made reuse of resistance elements among blocks. For accurate power integrity analysis, the DC simulation is not sufficient and the dynamitic simulation with capacitive and inductive models is required. However, the idea in [15] can not be directly applied to partial reluctance extraction, because the partial reluctance depends on environments and same geometry of P/G wires does not imply same partial reluctances.

In this paper, the structural regularity of the P/G grid is exploited with the consideration of locality property of partial reluctance. A comprehensive reuse scheme is proposed for large-scale P/G grid structures. Combined with an efficient extraction approach for frequency- dependent partial reluctance and resistance, the proposed method enables accurate inductive modeling of large-scale P/G structures. Numerical experiments on the regular P/G structures with up to one hundred thousands of wire segments show that, the proposed method is several to tens times faster than the window-based extraction method in [12]–[14], while preserving high accuracy. A remedy technique is proposed for the P/G structures with a little of irregularity. After identifying the wire segments changed from an original regular structure, we set them as aggressor conductors in turn to perform an additional reluctance extraction. Numerical results validate the efficiency of using the remedy technique.

2. Window-Based Partial Reluctance Extraction with High-Frequency Consideration

In this section, we firstly give an overview of the window-based extraction technique for partial reluctance extraction. The efficient method for the intra-window extraction of frequency-dependent reluctance and resistance is then described [14].

2.1 Overview of Window-Based Reluctance Extraction

Because the partial reluctance has the locality property, it is safe to ignore the mutual reluctance (K-element) between two conductors far from each other. A window-based method has been utilized to extract the reluctances [4]–[8], [10]–[14]. It includes the following steps:

1. For conductor i, select its nearby conductors and itself to form a coupling window W_i;
2. Calculate the mutual reluctances between conductor i and other conductors in W_i, while the mutual reluctances between conductor i and conductors outside the window is set to 0;
3. Execute the above steps for every conductor, and then fill these reluctances, column by column, into a global $\boldsymbol{K}$ matrix;
4. Generate a symmetric reluctance matrix through $\boldsymbol{K} := (\boldsymbol{K} + \boldsymbol{K}^T)/2$.

How to select the coupling window is a key point to assure the accuracy and efficiency of reluctance extraction. A larger window would bring high accuracy as well as long running time, and a smaller window would result in less accuracy. A window selection algorithm has been proposed based on the shield effect [6], which however was applied to 2-D aligned conductors. Based on some definitions in [6], a window selection method dealing with 3-D complex structures was proposed in [11]. This method considers both shield effect and distance among conductors, and is adopted in [12]–[14] and this paper.

Selecting the coupling window is actually choosing some nearby conductors for a specified aggressor conductor (the rest are called victim conductors). In [11], a coupling level is defined for each victim (the less the coupling level, the stronger coupling effect is). Then, all victims whose coupling level is less than a specified "max coupling level" and the aggressor itself form the window. For a general 3-D conductor alignment, the procedure of determining the victim's coupling level is performed with the conductor projections on the X-Y, Y-Z, and X-Z coordinate planes. In each plane, the projections are sorted in two directions at first to get two queues of projections. For each queue, the projection is set as aggressor in turn, and then the coupling levels of other projections are calculated according to the shield level and their distance. After executing the above procedure for all the six projection queues, the minimum of the coupling levels between two conductors is used as the final result.

With the high-frequency effect not considered, the reluctances within a window are obtained by inverting the inductance matrix, based on (1). While the high-frequency effect is considered, the conductors need to be meshed into filaments along the current direction. The current flowing in each filament is assumed to have uniform density, and then the frequency-dependent reluctance can be extracted. The flow of window-based reluctance extraction will not change, but the intra-window extraction (i.e. the 2nd step) would become complicated. The techniques for the intra-window extraction of frequency-dependent reluctance and resistance are introduced below [12]–[14].

2.2 Intra-Window Extraction Techniques Considering the High-Frequency Effect

For a window including N_c conductors, the relation between voltages $\boldsymbol{V}$ imposed on conductors and corresponding currents $\boldsymbol{I}$ is:

$$(\boldsymbol{R} + j\omega\boldsymbol{L})\boldsymbol{I} = \boldsymbol{V}, \tag{2}$$

where $\boldsymbol{V}, \boldsymbol{I} \in \mathbb{C}^{N_c}$, ω is angular frequency. $\boldsymbol{R}, \boldsymbol{L} \in \mathbb{R}^{N_c \times N_c}$ are the resistance matrix and the partial inductance matrix of conductors, respectively. Combining with (1), we have:

$$j\omega\boldsymbol{I} = \boldsymbol{K}(\boldsymbol{V} - \boldsymbol{R}\boldsymbol{I}). \tag{3}$$

If we set the i'th entry of $\boldsymbol{V} - \boldsymbol{R}\boldsymbol{I}$ to $j\omega$ and others to zero, then the resulting current distribution $\boldsymbol{I}$ would be equal to

the i'th column of $\boldsymbol{K}$ matrix. Then, it becomes the problem of calculating the current of the conductors under the condition:

$$\boldsymbol{V} - \boldsymbol{R}\boldsymbol{I} = j\omega \boldsymbol{e}_i. \tag{4}$$

Here $\boldsymbol{e}_i$ is a vector with N_c zeros, except the i'th entry being one.

Suppose the N_c conductors are meshed into N_f filaments in total to capture the high-frequency effect. The relation between filament voltages $\hat{\boldsymbol{V}}$ and currents $\hat{\boldsymbol{I}}$ can be expressed as:

$$(\hat{\boldsymbol{R}} + j\omega\hat{\boldsymbol{L}})\hat{\boldsymbol{I}} = \hat{\boldsymbol{V}}, \tag{5}$$

where $\hat{\boldsymbol{V}}, \hat{\boldsymbol{I}} \in \mathbb{C}^{N_f}$. $\hat{\boldsymbol{L}}, \hat{\boldsymbol{R}} \in \mathbb{R}^{N_f \times N_f}$ are partial inductance matrix and resistance matrix of filaments, which can be obtained by analytical formulas [2], [16].

We can define a mesh incidence matrix $\boldsymbol{M} \in \mathbb{R}^{N_c \times N_f}$, where $\boldsymbol{M}_{ik}$ is 1 when filament k is in conductor i, and 0 otherwise. Then, the filament current and voltage are related with conductor current and voltage through:

$$\boldsymbol{I} = \boldsymbol{M}\hat{\boldsymbol{I}}, \hat{\boldsymbol{V}} = \boldsymbol{M}^T\boldsymbol{V}. \tag{6}$$

Since $\boldsymbol{K}$ is a real matrix, the conductor currents must also be real under the condition (4). According to (6), we have:

$$\boldsymbol{I}_{im} = \boldsymbol{M} \cdot \hat{\boldsymbol{I}}_{im} = 0, \tag{7}$$

where $\hat{\boldsymbol{I}}_{im}$ is the imaginary part of $\hat{\boldsymbol{I}}$. Now, decomposing the real and imaginary parts of (5) and substituting (4) and (6), we have

$$\hat{\boldsymbol{R}}\hat{\boldsymbol{I}}_{re} - \omega\hat{\boldsymbol{L}}\hat{\boldsymbol{I}}_{im} = \hat{\boldsymbol{V}}_{re} = \boldsymbol{M}^T\boldsymbol{V}_{re}, \tag{8}$$

$$\omega\hat{\boldsymbol{L}}\hat{\boldsymbol{I}}_{re} + \hat{\boldsymbol{R}}\hat{\boldsymbol{I}}_{im} = \hat{\boldsymbol{V}}_{im} = \boldsymbol{M}^T\omega e_i. \tag{9}$$

Equations (7)–(9) can be combined to become a matrix equation:

$$\begin{bmatrix} \hat{\boldsymbol{R}} & -\omega\hat{\boldsymbol{L}} & -\boldsymbol{M}^T \\ \omega\hat{\boldsymbol{L}} & \hat{\boldsymbol{R}} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{M} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{I}}_{re} \\ \hat{\boldsymbol{I}}_{im} \\ \boldsymbol{V}_{re} \end{bmatrix} = \begin{bmatrix} \boldsymbol{0} \\ \omega\boldsymbol{M}^T\boldsymbol{e}_i \\ \boldsymbol{0} \end{bmatrix}. \tag{10}$$

This equation includes $N_c + 2N_f$ real equations and the same number of real unknowns. After solving it, we can obtain the conductor currents $\boldsymbol{I}$ through $\boldsymbol{I} = \boldsymbol{M}\hat{\boldsymbol{I}}$, that is the i'th column of matrix $\boldsymbol{K}$.

For densely coupled conductor system, the intra-window extraction including hundreds of filaments consumes a lot of CPU time. The techniques of equation condensation and rescaling were proposed in [12]–[14]. With them, the following equation is derived from (10) and solved by the GMRES algorithm [17]:

$$\begin{bmatrix} \boldsymbol{1}+(\omega\hat{\boldsymbol{R}}^{-1}\hat{\boldsymbol{L}})^2 & -\hat{\boldsymbol{R}}^{-1}\boldsymbol{M}^T \\ \omega\boldsymbol{M}\hat{\boldsymbol{R}}^{-1}\hat{\boldsymbol{L}} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \hat{\boldsymbol{I}}_{re} \\ \boldsymbol{V}_{re} \end{bmatrix} = \begin{bmatrix} \omega^2\hat{\boldsymbol{R}}^{-1}\hat{\boldsymbol{L}}\hat{\boldsymbol{R}}^{-1}\boldsymbol{M}^T e_i \\ \omega\boldsymbol{M}\hat{\boldsymbol{R}}^{-1}\boldsymbol{M}^T\boldsymbol{e}_i \end{bmatrix}, \tag{11}$$

where $\boldsymbol{1}$ stands for the identity matrix. Because $\hat{\boldsymbol{R}}$ is a diagonal matrix and matrix $\boldsymbol{M}$ is very sparse, the computational expense of this condensing procedure is very little. The rescaling with the angular frequency ω well balances the matrix entries, and guarantees fast and stable convergence of the GMRES algorithm [13], [14].

To calculate the frequency-dependent resistance, we consider the N_c conductors within window W_i. The relation between the voltage drop on conductors i and conductor currents is

$$V_i = \sum_{k=1}^{N_c} R_{ik}I_k + j\omega \sum_{k=1}^{N_c} L_{ik}I_k. \tag{12}$$

Under the condition (4), the currents I_k are real numbers (equal to reluctance). Then, decomposing the real and imaginary portions of (12), we have

$$\mathrm{Re}(V_i) = \sum_{k=1}^{N_c} R_{ik}I_k \approx R_{ii}I_i. \tag{13}$$

The approximation is due to two reasons. The first one is that the mutual resistance R_{ik} $(i \neq k)$ is nearly zero when the frequency is not ultra high; the second is that I_i is much larger than other I_k's since I_i equals to the self reluctance. So, the resistance can be calculated with

$$R_{ii} = V_{re,i}/I_i \tag{14}$$

where $V_{re,i}$ and I_i are obtained from the solution of (11). Thus, the frequency-dependent resistance is easily obtained, along with the reluctance extraction.

3. Extraction Techniques for the Regular P/G Grid Structure

In this section, the regular P/G grid model is firstly introduced. Then, a reuse technique taking advantage of the structural regularity is proposed for reluctance extraction. Finally, the limitation of the reuse technique is discussed and a remedy for irregular P/G structures is presented.

3.1 The Regular P/G Structure

Usually, a P/G grid is routed on different metal layers of a VLSI chip using mass metal resources to form a mesh structure [15]. In each layer, the orientation of metal wires is along either the X-axis or Y-axis, alternatively. And, the power wires are interlaced with the ground wires. Between two adjacent layers, the P/G wires are connected through vias, which cut the wires into small metal segments. Figure 1 shows the 3-D view of a small-size two-layer P/G grid.

In many cases, the P/G grid has a certain regularity of geometry. It is always designed to be a regular one in early design stage, which means that in a certain metal layer, each metal wire has the same width, and the pitch between two wires is also identical [15]. Further, because the vias can only be laid down at the places that the upper metal wires intersect with the lower wires, the evenly distributed metal wires make the evenly distribution of vias. Besides that for the early-stage design, this regular P/G structure can also

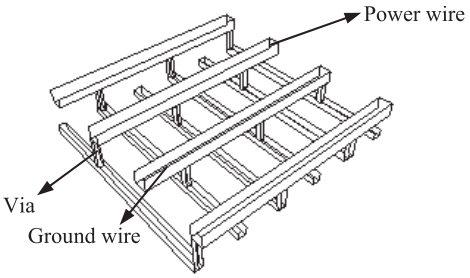


Fig. 1 A two-layer structure of P/G grid.

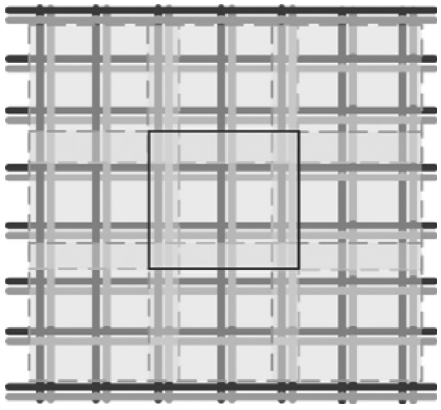


Fig. 2 The P/G grid is partition with overlapped blocks [15].

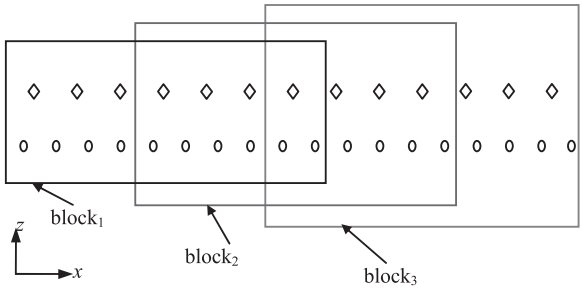


Fig. 3 The *X*-*Z* plane view of two-layer P/G wires, where three blocks along *X*-axis are defined.

present for some circuit module, as a part of the whole-chip P/G grid.

3.2 Basic Idea of Block Reuse

Shi et al. proposed a pattern idea to accelerate the DC simulation of P/G grids [15]. It explores the geometry characteristics of regular P/G grids and translates topology similarity to sub-matrix regularity. They divided the whole P/G grid into blocks on the *X*-*Y* plane (see Fig. 2), and made reuse of resistance elements among blocks. This idea is extended for reluctance extraction, which enables the inductive modeling and extraction of large-size P/G grids.

Because the mutual impedance or inductance of perpendicular conductors is negligible, the reluctance interaction among metal wires in the same direction is considered.

m: the number of layers of Y-direction P/G wires;
N_i: the number of P wires in the i'th layer;
p_i: the wire pitch between adjacent P wires in the i'th layer;
d_i: the number of P wires between the left boundaries of adjacent blocks in the i'th layer;
h: the threshold distance for locality judgement. If the distance of two parallel wires is larger than h, the mutual reluctance between them can be ignored.
l_i: the number of P wires in the i'th layer corresponding to the locality threshold distance: $l_i = \lceil h / p_i \rceil$;
n: the number of blocks along the X-axis;
n_i: the number of P wires in the i'th layer of a block.

Fig. 4 The notations for describing the block division of *Y*-direction P/G wires.

Without loss of generality, we consider the reluctance extraction for P/G wires along the *Y*-axis and describe the block partition along the *X*-axis. Figure 3 shows the side view of two-layer *Y*-direction P/G wires for extraction. For distinction, the wires on different layers are denoted by diamond and ellipse marks. We assume the power wire (P wire) and ground wire (G wire) always appear in pairs and their distance is the same. Therefore, in Fig. 3 and later illustrations we only plot the P wires to describe the block reuse technique.

In Fig. 3, the P/G wires are divided into three overlapped blocks. The geometric structure of conductors in each block is identical. Because of the locality of reluctance, we need not extract the mutual reluctance between two conductors far from each other. So, the structure of the leftmost block can be used for extracting the reluctance parameters of many segments in it. Due to the geometry identity among blocks, the results from the leftmost block can be reused for reluctances of segments within other blocks. With careful setting of block position and size, the error induced by reuse may be very limited. This technique, like a compact model, will greatly reduce the time and space consumption of the reluctance extraction for large P/G grids.

After handling the P/G wires along the *Y*-axis, the wires along the *X*-axis can be handled with similar procedure, which results in block partition along the *Y*-axis. Therefore, the P/G grid is divided into blocks on the *X*-*Y* plane (like that shown in Fig. 2). With the reuse of reluctance among blocks, the reluctance matrices for the *X*-direction and *Y*-direction P/G wires are efficiently generated, respectively. Their results are then combined to obtain a whole reluctance matrix. If the high-frequency effect is considered, the segment resistance is also influenced by environments. The techniques presented in Sect. 2.2 can be utilized along with the block reuse to get the frequency-dependent resistances.

3.3 Determine the Position and Size of Blocks

We consider the *Y*-direction P/G wires and describe how to partition the blocks in the *X*-*Z* plane. The related notations are listed in Fig. 4.

Suppose the P/G grid includes m Y-direction layers, where the metals are routed along the Y-axis. On the i'th layer ($i = 1, 2, \ldots, m$), the number of P wires is N_i and the center-to-center distance of adjacent two P wires is p_i (i.e. wire pitch). The P wires are numbered from 1 to N_i. Suppose the P/G structure is divided into n blocks along the X-axis (like that shown in Fig. 3), and the blocks are denoted by block_1, block_2, ..., block_n, from left to right. We can just take P wires into account when defining the blocks, and each G wire belongs to the block where its left neighbor P wire belongs to.

Because the wire width and pitch have different values for different layers, there is misalignment of P/G wires among different layers. We need to define an appropriate block distance to make the geometry misalignment as small as possible. Consider a set S:

$$S = \left\{ d \in \mathbb{N} \mid dp_m - \left\lfloor \frac{dp_m}{p_i} \right\rfloor p_i \leq \delta p_i,\ \forall i = 1, 2, \ldots, m-1 \right\}, \quad (15)$$

where δ is a threshold value, such as $\delta = 0.02$. The positive integer d in set S makes dp_m approximate the common multiple of the pitches of different layers. We let

$$d_m = \min(S), \quad (16)$$

which makes $d_m p_m$ the minimum common multiple, and define:

$$d_i = \lceil d_m p_m / p_i \rceil, \quad i = 1, 2, \ldots, m. \quad (17)$$

d_i stands for the number of P wires between the left boundaries of two adjacent blocks in the i'th layer. According to the definition,

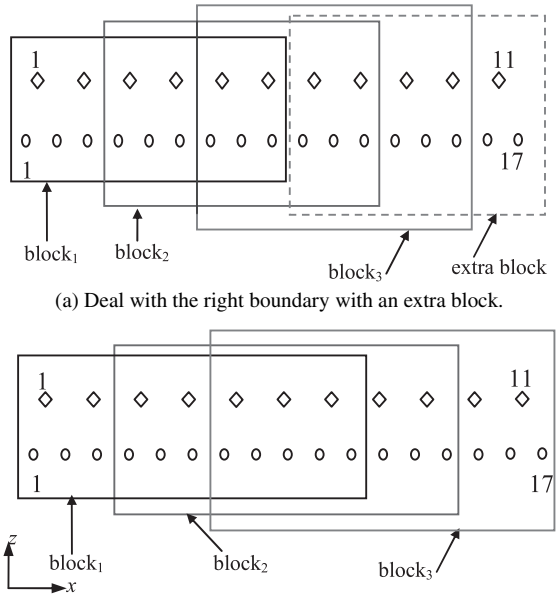
$$d_m p_m \approx \ldots \approx d_2 p_2 \approx d_1 p_1. \quad (18)$$

With a small δ value, this approximation induces little error. The average value of $d_i p_i$ is defined as the distance of two adjacent blocks. With this definition, the relative positions of P wires near the left boundary of the block are almost the same. For any two blocks including the same number of P wires, their inner structures are almost the same as well (as shown in Fig. 3). This enables the reuse of frequency-dependent reluctance and resistance among different blocks.

To determine the size of block is actually to choose the number of P wires that a block includes. Thanks to the locality effect of reluctance, only nearby environment conductors must be included. Suppose there is a threshold distance h, and the mutual reluctance becomes negligible if the distance of two parallel conductors is larger than h. In the i'th layer, we use n_i to denote the number of P wires in a block. Because the wires from 1 to d_i are only in block_1, the reluctances of wire d_i must be extracted with the structure of block_1. If defining

$$l_i = \lceil h / p_i \rceil, \quad (19)$$

we have $n_i \geq d_i + l_i$, to keep all the nearby conductors of wire d_i within block_1. To make the reluctances of wire $d_i + l_i$ extracted within block_1, we let $n_i = d_i + 2l_i$. Now, the wire $d_i + l_i + 1$ is at least h far from the left boundary of block_2, so that its reluctances can be extracted with the structure of block_2. For the same reason, the reluctances of wires $d_i + l_i + k$ ($k = 2, \ldots, l_i$) can also be extracted within block_2.



(a) Deal with the right boundary with an extra block.

(b) Deal with the right boundary by enlarging the block size.

Fig. 5 Two approaches to handle the P/G wires near the right boundary.

With the block size $n_i = d_i + 2l_i$, we can define block_2, block_3, and so on. Now, we look at the rightmost P/G wires. If the number of P wires $N_i = nd_i + 2l_i$, all P wires are contained in the n blocks. All blocks have the same size and no additional operation is needed. Otherwise, there are some P wires outside the blocks, as shown in Fig. 5. One way to handle this scenario is to add an extra block for extracting reluctances of P/G wires near the right boundary, as shown in Fig. 5(a). However, this causes two blocks of structure simulated with the complicated extraction algorithm. A more efficient way is to increase the size of block. If the number of P wires in a block becomes:

$$n_i = N_i - nd_i + d_i, \quad (20)$$

where

$$n = \left\lfloor \frac{N_i - 2l_i}{d_i} \right\rfloor, \quad (21)$$

all P/G wires are contained in the n blocks with same size. And because each block includes more wires, the accuracy will not decrease. With this technique, we can only extract one block and make reuse of reluctance for all wires. This manipulation of boundary is shown in Fig. 5(b).

Figure 6 gives the X-Z plane view of Y-direction P wires in a larger P/G structure. For this example, the numbers of P wires in two layers are $N_1 = 36$ and $N_2 = 26$. The pitches are $p_1 = 2.4\,\mu$m and $p_2 = 3.2\,\mu$m, respectively. With (15)–(17), we obtain $d_1 = 4$ and $d_2 = 3$. We assume $h = 15.0\,\mu$m to characterize the locality property of reluctance.

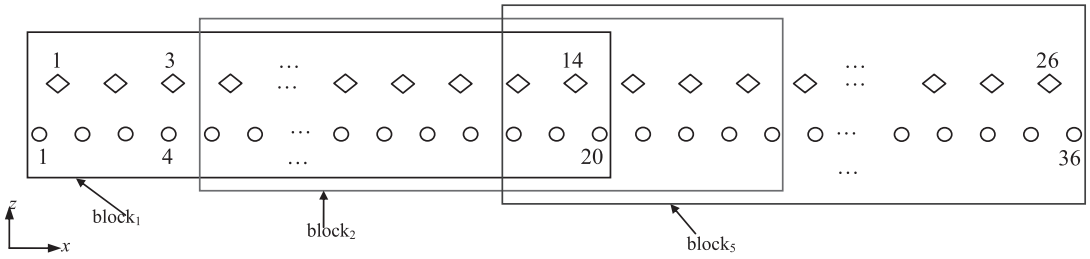


Fig. 6 The *X*-*Z* plane view for a larger P/G grid structure.

Then, $l_1 = 7$ and $l_2 = 5$, according to (19). We calculate the number of blocks $n = 5$ from (21), and the block size becomes $n_2 = 14$ (or $n_1 = 20$). For the *Y*-*Z* plane view of this structure, the corresponding parameters for block division can be determined similarly. Finally, we only need to extract reluctances for one block, and the results are reused to obtain the whole reluctance matrix.

3.4 Assemble the Extraction Results

Because all blocks have the same inner structure, the reluctance matrix for block_1 can be reused by other blocks. For each P/G wire, we shall firstly determine which block it belongs to for extracting reluctance. Take the structure in Fig. 5(b) as an example. The two-layer *Y*-direction P/G wires are divided into three blocks, and each block contains 7 upper-layer P wires and 11 lower-layer P wires. The reluctances of the P wires from 1 to 4 in the upper-layer and the wires from 1 to 6 in the lower-layer are extracted within block_1. The reluctance matrix for structure in block_2 provides the reluctances of wires 5 and 6 in the upper layer and the wires from 7 to 9 in the lower layer. The reluctance matrix for structure in block 3 provides the reluctances of wires from 7 to 11 in the upper layer and the wires from 10 to 17 in the lower layer.

For a general case, we introduce how to obtain the reluctances from appropriate blocks. Take the reluctance couplings among P wires in a one-layer structure as an example. For the P wire s in the i'th layer, the following reluctances of s are calculated, considering the locality effect:

$$\begin{cases} K_{s,s}K_{s,s+1}\ldots K_{s,s+l_i}, & \text{if } 1 \le s < N_i - l_i \\ K_{s,s}K_{s,s+1}\ldots K_{N_i}, & \text{if } N_i - l_i \le s \le N_i \end{cases}.$$

To determine in which block these reluctances are extracted, we obey the following rules:

- If $1 \le s \le d_i + l_i$, the conductors which has reluctance coupling with conductor s are all in block_1. So, the reluctances of conductor s are extracted in block_1;
- If $(k-1)d_i + l_i + 1 \le s \le kd_i + l_i$, $(k = 2, 3, \ldots, n-1)$, the reluctances of conductor s are extracted in block_k;
- If $(n-1)d_i + l_i + 1 \le s \le N_i$, the reluctances of conductor s are extracted in block_n.

Assembling the results for different values of s, we can easily have a symmetric reluctance matrix $\boldsymbol{K}$.

For the coupling between P wires and G wires, and between P/G wires in different layers, the judgment is just similar. The rules determining the appropriate block can be derived for all P/G segments in the multi-layered structure. Note that the reluctance matrix for each block is the same, and the whole reluctance matrix can be assembled with little computational expense.

3.5 Algorithm Flow and Analysis

The proposed algorithm is summarized as follows:

Step 1. Process the *X*-direction P/G wires to determine the block division from the *Y*-*Z* plane view with the technique in Sect. 3.3; Process the *Y*-direction P/G wires similarly. Then, obtain the blocks on the *X*-*Y* plane.

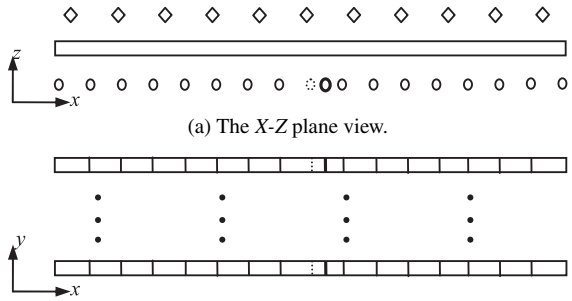
Step 2. Extract the reluctances for the *X*-direction wires and *Y*-direction wires within the center block from the *X*-*Y* plane view, respectively. This utilizes the techniques presented in Sect. 2. For high frequency, both reluctance and resistance are obtained.

Step 3. Assemble the extraction results based on the rules in Sect. 3.4, to obtain two global matrices, one for the *X*-direction wires and the other for the *Y*-direction wires; the two matrices can be combined to have a whole reluctance matrix for the P/G grid structure.

Compared with the window-based extraction method, the proposed algorithm only handles the aggressor conductors within one block. Assuming the same computational time of reluctance extraction for each aggressor, the speedup ratio of the proposed algorithm would approximate the ratio of the number of segments in the whole P/G grid over the number of segments in a block. For an arbitrary set of wire pitches $p_1, p_2, \ldots, p_m$, the d_m obtained from (16) may be very large. This means the size of block is large and the speedup of the proposed method to the window-based extraction method would become limited.

3.6 Handle Irregular P/G Structures

In later design stages, the on-chip P/G grid is often not as regular as that in early design stage. Designers always make tiny changes anywhere they think suitable to fix the power supply problems [15]. For an irregular P/G structure, the proposed method is not applicable. Below, we introduce a remedy technique for the irregular structure derived from a



(a) The *X*-*Z* plane view.

(b) The *X*-*Y* plane view of the layer above the changed wire.

Fig. 7 An example of the little change on a regular P/G structure.

little change on a regular P/G structure.

If only a few of wires in the regular structure are removed, inserted, or changed on position or width, we can perform an additional reluctance extraction for the changed wire segments. Then, the obtained reluctances are substituted for those extracted from the regular structure. Figure 7 shows an example of the little change on a regular P/G structure. Suppose a P wire at the lowest layer (shown as a bold ellipse) is widened and moved away. This affects the wire itself and the segmentation of the P wires above it (see Fig. 7(b)). In addition to those on the moved wire, there are two changed segments for each P wire in the above layer. These changed segments are set as the aggressor in turn, for performing the additional reluctance extraction. In this example, the wire is moved along the *X*-axis, and the structural regularity along the *Y*-axis is not affected. Thus, with the block reuse along the *Y*-axis, the number of aggressor segments for extraction can be further reduced.

For a general structural change on a regular P/G grid, we can determine the affected P/G segments similarly. After an extra extraction for the affected segments, the reluctance matrix of the whole structure can be corrected accordingly. Providing the irregular structure is derived from a little change on a regular P/G structure, the affected segments would be much fewer than those in the whole structure. In this case, the remedy technique combined with the proposed reuse method would achieve high efficiency for reluctance extraction. Because the reluctance between two unchanged segments varies little, the proposed method usually has sufficient accuracy.

4. Numerical Results

The proposed algorithm has been implemented as PG_extractor, a program written in C language for frequency-dependent reluctance and resistance extraction considering the regular P/G grid structure. The numerical experiments are performed on a Sun Fire V880 server with 750 MHz CPU. The results of PG_extractor are compared with the DRRE (direct reluctance and resistance extraction) algorithm in [14] and the impedance extractor FastHenry [18] developed by MIT.

Four P/G grid structures with four layers of wires are used to demonstrate the accuracy and efficiency of the proposed method. In the first case, each of the upper two layers includes 10 P wires and 10 G wires, and the wire pitch is 6.36 μm. For the lower two layers, each includes 16 P wires and 16 G wires, with wire pitch of 4.23 μm. The vias between adjacent layers cut the wires into segments. The first case includes 1830 segments in total. The other three cases have similar structure, but with different wire pitches and number of wires. Their segment numbers are 4810, 11156 and 102674, respectively. We assume the threshold distance h for locality of reluctance is $h = 12\,\mu$m. Besides, to capture the high-frequency effect at 10 GHz, each segment in the upper two layers is partitioned into 3×3 filaments.

Table 1 Error distribution of loop inductance for the fist case.

	Error distribution of loop inductance (%)		
	<3%	3%-6%	>6%
PG_extractor vs FastHenry	95.1	4.8	0.1
DRRE vs FastHenry	98.7	1.3	0
PG_extractor vs DRRE	98.9	1.1	0

Table 2 Computational time for the four cases. (Unit in second)

Case	Segment #	FastHenry	DRRE	PG_extractor	Speedup
1	1830	8856	55.6	18.5	3.0
2	4810	--	109.9	19.2	5.7
3	11156	--	428.7	41.9	10
4	102674	--	5034.6	109.2	46

The proposed algorithm divides the first P/G structure into 3×3 blocks on the *X*-*Y* plane. Each block contains 6 P wires and 6 G wires for the upper two layers and 10 P wires and 10 G wires for the lower two. Then, PG_extractor invokes DRRE to extract the center block, and the results are reused to obtain the whole reluctance matrix and resistance matrix. The reluctance matrix is inversed to the inductance matrix, and the loop inductance of any two segments is compared with that from FastHenry's results. It is fair to compare the loop inductance while evaluating the accuracy of inductive modeling [4]. Table 1 lists the error distribution of loop inductance for the first case. The maximum error to FastHenry's result is 8.5%. For the resistance, the maximum error is within 5%.

In the second case, each of the lower two layers includes 25 P wires and 25 G wires, and each upper layer includes 17 P wires and 17 G wires. PG_extractor divides the structure into 6×6 blocks. Because so many conductors are involved, FastHenry can not calculate the inductance matrix for this case. We can just compare the results from PG_extractor and DRRE. The comparison show that the differences in loop inductance are all within 6%, and 99% of loop inductances have discrepancy within 3%. For two larger cases, the dimension of inductance matrix is so large that the matrix inversion is difficult. This prohibits the comparison between PG_extractor and DRRE.

For the four test cases, the CPU time of the three methods are listed in Table 2. The speedup is with respect to DRRE. FastHenry is not able to extract the impedance for

the three larger cases, due to the limitation of CPU time and memory usage. From the table, we can see that the speedup of PG_extractor to DRRE varies from three to 46 with the size of the P/G structrue increasing.

To evaluate the efficiency of the technique proposed in Sect. 3.6, an irregular P/G structure is constructed through modifying the first case. One P wire in the lowest layer is moved for a distance equal to 10% of the pitch, while its width is decreased by 10% (the scenario is similar to that in Fig. 7). The additional extraction is performed with 29 P wire segments set as aggressor (the block reuse along the Y-axis is considered), and its results are used to replace the corresponding entries in the reluctance matrix. The experimental results are compared with the results of FastHenry, which shows the error distribution of loop inductance is hardly worse than those in Table 1. For this irregular structure, there is 94.4% of loop inductances whose error is less than 3%. The number of loop inductances with above 6% error only accounts for 0.1%. The additional extraction consumes about 1 second of CPU time. This means for this slightly changed structure, the computational time for reluctance extraction is only increased by 5%.

5. Conclusions

An efficient method of frequency-dependent partial reluctance extraction is developed for the large-scale P/G structure. The regularity of the P/G grid is exploited by a technique of block division, which produces blocks with similar inner structure. Then, efficient window-based extraction technique is used to obtain the reluctance and resistance of one block, whose results are reused for the other blocks and finally assembled for the whole reluctance matrix. Numerical results demonstrate the proposed method is able to handle large-scale P/G structures with high accuracy and efficiency.

For the P/G structures with a little of irregularity, a remedy technique is proposed to correct the reluctance matrix extracted from a corresponding regular P/G structure. The preliminary results of using the remedy technique validate its efficiency. While performing reluctance extraction for a general irregular P/G structure, the regularization technique as used for DC analysis [15] may not work. Extending the proposed method for general irregular P/G grids, including considering the regularization technique, could be explored in the future.

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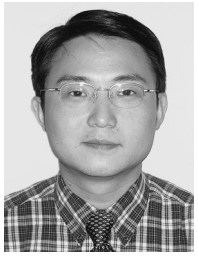

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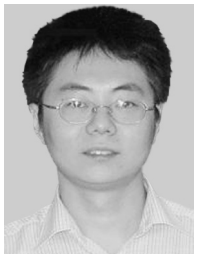

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