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Accurate Eye Diagram Prediction Based on Step Response and Its Application to Low-Power Equalizer Design

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SUMMARY This paper introduces a step response based method to predict the eye diagram for high-speed signaling systems. The method is able to predict accurately the worst-case eye diagram, and is orders of magnitude faster than the method using SPICE simulation with input of random bits. The proposed method is applied to search optimal equalizer parameters for lower-power transmission-line signaling schemes. Simulation results show that the scheme with driver-side series capacitor achieves much better eye area, and signaling throughput than the conventional scheme with only resistive terminations.

key words: *eye diagram, jitter, lossy transmission line, step response*

1. Introduction

To evaluate the signal quality of high-speed serial communication, an eye diagram is produced to provide the most fundamental and intuitive view. Two metrics are used to characterize the eye diagram: eye-opening voltage and timing jitter. The traditional method to predict the eye diagram involves performing time-domain transient simulation. To shorten the simulation time, a limited length of pseudo-random bit sequence (PRBS) is usually used as the input stimulus, but it can hardly result in the worst case for many high-speed signaling systems. Therefore, an accurate and efficient method for predicting the eye diagram will be very helpful, and can enable fast and comprehensive design space exploration.

In [1], Casper et al. developed the peak distortion analysis method to predict the worst-case eye-opening voltage from the unit pulse response of the system. This method considers all interference sources and avoids tedious transient simulation. In [2], [3], the performance of on-chip transmission line was investigated, and an analytical formula was proposed to estimate the maximum eye-opening voltage. The formula was derived from a piecewise-linear eye model and assumed the far-end voltage reaches V_{dd} when time $2t_{tof}$ passed after rising, where t_{tof} is the time-of-flight. Zhu et al. [4] assumed the step response is a bitonic waveform, and extracted five pivotal points on the step response to predict the eye-opening voltage. However, the bitonic assumption does not hold for general signaling schemes. In [5], Analui et al. proposed analytical techniques to estimate jitter based on step response and unit pulse response. The jitter distribution and the impact of each prior bit were also investigated.

Off-chip interconnect design is important to improve the overall system performance [6]. For high-speed off-chip interconnect, inter-symbol interference (ISI) is a major obstacle of performance due to the frequency-dependent propagation characteristics of transmission line. A usual measure for suppressing ISI is to add pre-emphasis at the driver side and equalization at the receiver side. Recently, the transmission line with simple passive terminators has been studied [2], [4]. These schemes have much lower power consumption than the schemes with active pre-emphasizer or equalizer.

In this paper, we extend the idea in [4] by considering a general step response, and propose an accurate method to predict the worst-case eye diagram. The step response based method extracts the eye opening and timing jitter without time-consuming SPICE simulation of long input bit patterns. It also generates the input bit patterns which produce the worst-case inter-symbol interference. The proposed method is applied to lower-power equalizer design for off-chip transmission line. For a scheme with only termination resistor and a scheme with driver-side series capacitor, the prediction method is utilized to efficiently explore the design space and find the optimal design parameters. Compared with the SPICE simulation using long random input patterns, the proposed method demonstrates much higher accuracy and is orders of magnitude faster. The simulation results suggest that the driver-side capacitor scheme has large advantage over the conventional termination scheme, in performance metrics like eye area and signal throughput, while not increasing power consumption.

It should be pointed out that the step response based method is equivalent to the peak distortion analysis [1] for signals with fixed bit rate. However, the step response is more fundamental, and implicates certain characteristics of the system, such as the time-of-flight delay and reflection and saturation voltages of transmission line signaling. Therefore, the proposed method is more extensible and suitable for design space exploration. Moreover, a step response can be used to estimate the eye diagrams for various signal bit rates if assuming the signal rise/fall time unchanged.

In Sect. 2, the relationship between transient response for an arbitrary input signal and the step response is introduced, followed by the description of eye diagram. The step

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response based method to predict the worst-case eye diagram is proposed in Sect. 3. Section 4 includes simulation results to validate the proposed method. Then, an application of low-power equalizer design for off-chip signal transmission is discussed. The last section concludes this paper.

2. Preliminaries

For linear time-invariant (LTI) signaling system, the transmitted digital signal can be modeled as a linear combination of time shifted step responses. Hence, the eye diagram can be analyzed based on the step response of the signaling system.

2.1 The Step Response and Response for Arbitrary Digital Input

The step response defines the time behavior of the system's output when the input changes from zero to one in a very short time (rise time). Figure 1 shows a step input waveform and the corresponding step responses for a transmission line when different terminations are applied. From Fig. 1, it is obvious that the bitonic assumption in [4] is not always hold. And, we can clearly see the time-of-flight delay, the reflection and the saturation voltage. It may be easy to explain the impact of pre-emphasizer or equalizer on the step response, as well.

If the rise time and fall time of digital signals are assumed to be the same, the system's input can be modeled with a linear combination of step inputs. Then, the transient response of an arbitrary input signal can be formulated with the step response.

Let us denote the step response as $s(t)$:

$$\begin{cases} s(t) = 0, \ t \le 0 \\ s(t) > 0, \ t > 0 \end{cases}. \tag{1}$$

To simplify the notation, the output time is implicitly shifted by the time-of-flight. In other words, we shift the origin of time axis at output to the time when the step response starts rising from zero. Since our derivation is concerned about the eye diagram, the shifting does not hamper the validity of the results.

We assume the system is linear time invariant. The input is determined by the direction and position of all signal transitions, i.e. a stream $\mathrm{B} = \{b_i, w_i\}_{i=0}^{\infty}$. Here b_i and w_i stand for the direction and position of the ith transition, respectively. Thus, using the principle of linear superimposition, we can express the system's output $y(t)$ as:

$$y(t) = \sum_{i=0}^{\infty} b_i \cdot s(t - w_i T), \tag{2}$$

where T is the bit width, i.e. the clock cycle time. The two sequences $\{b_i\}_{i=0}^{\infty}$ and $\{w_i\}_{i=0}^{\infty}$ fulfill:

$$b_0 = 1, \ b_{i+1} = -b_i, \tag{3}$$

$$w_0 \ge 0, \ w_{i+1} = w_i + d_i. \tag{4}$$

Here d_i is the number of consecutive bits of $(b_i + 1)/2$ in the input signal. Since the ith signal transition happens at time $w_i T$, and sequence $\{w_i\}_{i=0}^{\infty}$ is an increasing sequence. Note that the upper bound of sequence index is ∞, because we may consider signal with infinite length for the worst case of eye diagram.

2.2 Eye Diagram Description

The eye diagram is generated by overlapping the transient response $y(t)$ on a fixed time window of multiple cycle periods, as shown in Fig. 2. Several system performance measures can be derived from the eye diagram. The eye opening, denoted by V_{EYE}, is the measure of the additive voltage noise in the signal. The eye width, denoted by t_{TJ}, is the measure of timing jitter effects. With these two parameters, we can model the area of eye opening with following approximate formula:

$$AREA_{EYE} = V_{EYE} \cdot (T - t_{TJ})/2. \tag{5}$$

Below we confine our discussion to the worst case situation, which leads to an eye diagram with the maximum timing jitter and minimum eye opening. We first present a theorem revealing the symmetry property of eye diagram at the worst case.

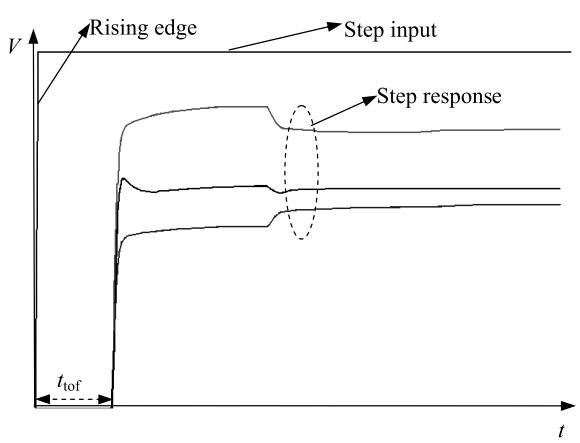


Fig. 1 The step input and corresponding step responses.

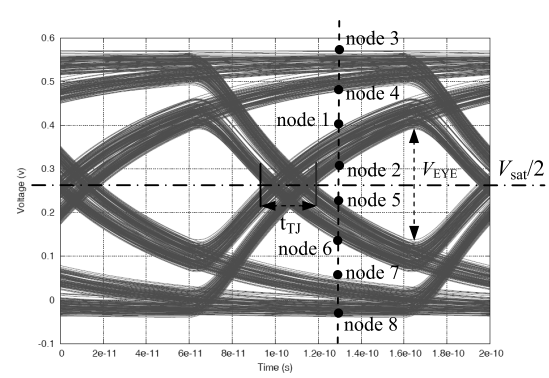


Fig. 2 An eye diagram, with eight voltage bounds for any time point.

Theorem 1: There exists an input bit pattern, which causes a symmetric eye diagram with the maximum timing jitter and minimum eye-opening voltage. And, the symmetric pivot is $V = V_{sat}/2$, where V_{sat} is the saturation voltage of step response.

Proof: We prove the theorem by construction. Given an input stream B, we append it a stream representing a zero-one transition holding until the step response saturates. Then, a stream –B is shifted and appended afterward, where minus sign indicates that all bit b_i in B is negated. Thus, the output contributed by stream –B mirrors on the original output along the horizontal line of $V = V_{sat}/2$. Consequently, a composite eye diagram is symmetric along $V = V_{sat}/2$.

Above deduction shows that for any input B, we can modify it to make the resulted eye diagram symmetric. Therefore, the eye diagram at the worst case must also be symmetric, with the pivot of $V = V_{sat}/2$. **End of proof**.

The step response based method we developed calculates the signal distortion from inter-symbol interference and predicts the worst-case eye diagram. In our analysis, the eye diagram is created by overlapping the signal waveform in the time window of one symbol period T. There are eight voltage bounds for every time point in the eye diagram, denoted by bold dots in Fig. 2. Node 1 and node 2 are '1' edge rising upper and lower bounds respectively, representing the maximum and minimum voltage for zero to one transition. Node 3 and node 4 are '1' edge holding upper and lower bounds respectively, representing the maximum and minimum voltage for continuous one bits. The other four nodes are '0' edge falling upper and lower bounds, and '0' edge holding upper and lower bounds.

These eight voltage bounds for all the time points in the overlapping time window will capture all the valuable features of the eye diagram.

3. Worst-Case Eye Diagram Prediction

Based on the step response, the '1' edge rising upper and lower bounds for worst-case eye diagram are first evaluated. With them, the eye opening and timing jitter can then be calculated due to the symmetry of eye diagram.

3.1 '1' Edge Rising Upper and Lower Bounds

Since the eye diagram is created by overlapping the signal waveform in the time window of T, the waveform in the eye diagram can be given by:

$$e(t) = \begin{cases} y(t) \\ y(t+T) \\ \cdots \\ y(t+kT) \\ \cdots \end{cases}, t \in [0, T] \tag{6}$$

For an observing time point t_0, $e(t_0)$ includes the values of $y(t_0+kT)$, where k is a non-negative integer. From (1) and (2), we have

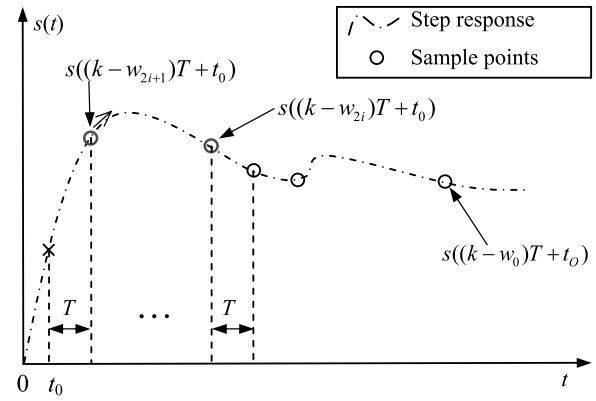


Fig. 3 A general step response $s(t)$, and the sampling points contributed to ΔV. To make ΔV minimum, both $s((k-w_{2i})T+t_0)$ and $s((k-w_{2i+1})T+t_0)$ must belong to a decreasing stage.

$$y(t_0 + kT) = \sum_{i=0}^{n} b_i \cdot s(t_0 + kT - w_i T). \tag{7}$$

where n is the number of signal transitions in the time interval from 0 to kT. To derive the '1' edge rising upper and lower bounds, we assume the zero to one transition happens at time $t = kT$. Therefore, $b_n = 1$ and $w_n = k$. So,

$$y(t_0 + kT) = \sum_{i=0}^{n-1} b_i \cdot s(t_0 + kT - w_i T) + s(t_0). \tag{8}$$

Because $s(t_0)$ is a fixed value, we need only to know the lower bound and upper bound of

$$\Delta V = \sum_{i=0}^{n-1} b_i \cdot s((k - w_i)T + t_0), \tag{9}$$

where input stream $\{b_i,\ w_i\}_{i=0}^{n-1}$ and parameter n are the variables. The items in summation of (9) are values of step response at time point multiple T's away from t_0, which are denoted by the hollow circles in Fig. 3. These candidate voltages are from a sequence,

$$Y^{(t_0)} = \{s(T + t_0), s(2T + t_0), \cdots, s(kT + t_0)\}, \tag{10}$$

since $w_i \geq 0$, $i = 0, \ldots, n-1$ is an increasing sequence.

Note that for any input stream, n must be an even number, because $b_n = 1$ and the definition of $b_0 = 1$ in (3). Therefore, $b_{2i} = 1$, $b_{2i+1} = -1$, $i = 0, \cdots, n/2 - 1$.

Figure 3 shows a step response and the sequence $Y^{(t_0)}$. The waveform includes several interlaced monotonic increasing stages and monotonic decreasing stages. So does sequence $Y^{(t_0)}$. For example, if

$$Y^{(t_0)} = \{1.0, 1.2, 0.9, 0.7, 0.6, 0.65, 0.6, 0.55\},$$

{1.0, 1.2} and {0.6, 0.65} are the increasing sub-sequences and {1.2, 0.9, 0.7, 0.6} and {0.65, 0.6, 0.55} are the decreasing sub-sequences.

We count the decreasing sub-sequences from left to right. For the ith decreasing sub-sequence, we record its

starting and ending numbers as $V_{d\_\max,i}$ and $V_{d\_\min,i}$. Likewise, for the increasing sub-sequence, we record its starting and ending numbers as $V_{i\_\min,i}$ and $V_{i\_\max,i}$. For a given pair $(V_{d\_\max,i}, V_{d\_\min,i})$, we denote their indexes in sequence $Y^{(t_0)}$ be $(w_{d\_\max,i}, w_{d\_\min,i})$. Likewise, for a given pair $(V_{i\_\min,i}, V_{i\_\max,i})$, we denote their indexes in sequence $Y^{(t_0)}$ be $(w_{i\_\min,i}, w_{i\_\max,i})$. Thus, by definition, we have the step response $s(w_{d\_\min,i}T + t_0) = V_{d\_\min,i}$, and $s(w_{d\_\max,i}T + t_0) = V_{d\_\max,i}$. Likewise, $s(w_{i\_\min,i}T + t_0) = V_{i\_\min,i}$ and $s(w_{i\_\max,i}T + t_0) = V_{i\_\max,i}$.

The decreasing sub-sequences contribute to the lower bound of $y(t_0 + kT)$, i.e. the '1' edge rising lower bound. The extreme case can be derived from the pairs $(V_{d\_\max,i}, V_{d\_\min,i})$. The following theorem states this lower bound.

Theorem 2: The '1' edge rising lower bound for the worst case is:

$$y_{\min}(t_0 + kT) = \sum_{i=1}^{m} (V_{d\_\min,i} - V_{d\_\max,i}) + s(t_0), \qquad (11)$$

where m is the number of decreasing sub-sequences in $Y^{(t_0)} = \{s(T + t_0), s(2T + t_0), \cdots, s(kT + t_0)\}$.

Proof: We first show the existence of the bound and then demonstrate that the bound is the extreme case.

Existence of the bound: We construct the input stream with $(b_0, w_0) = (1, k - w_{d\_\min,m})$, $(b_1, w_1) = (-1, k - w_{d\_\max,m})$, and $(b_{2i}, w_{2i}) = (1, k - w_{d\_\min,m-i})$, $(b_{2i+1}, w_{2i+1}) = (-1, k - w_{d\_\max,m-i})$, $i = 1, \ldots, m - 1$. Because the indexes of $(V_{d\_\max,i}, V_{d\_\min,i})$ in sequence $Y^{(t_0)}$ are $(w_{d\_\max,i}, w_{d\_\min,i})$, the constructed input has a zero-one transition at the $k - w_{d\_\min,i}$ bit and a one-zero transition at the $k - w_{d\_\max,i}$ bit. They contribute $(V_{d\_\min,i} - V_{d\_\max,i})$ to ΔV. Therefore, the constructed input contribute $\sum_{i=1}^{m} (V_{d\_\min,i} - V_{d\_\max,i})$ to ΔV. Combining the last transition: $b_n = 1$ and $w_n = k$, we get the input signal which has output:

$$y(t_0 + kT) = \sum_{i=1}^{m} (V_{d\_\min,i} - V_{d\_\max,i}) + s(t_0).$$

The worst case of the bound: We examine the voltage contribution of the negative transition $b_{2i+1} = -1$ and positive transition $b_{2i} = 1$ to ΔV. From (9), the contribution is $s((k - w_{2i})T + t_0) - s((k - w_{2i+1})T + t_0)$, the difference between two items in sequence $Y^{(t_0)}$. Note that $(k - w_{2i}) > (k - w_{2i+1})$. If both items belong to an increasing sub-sequence in $Y^{(t_0)}$, they contribute a positive value to ΔV. We shall remove these two transitions from the input to reduce ΔV. If the $(k - w_{2i})$ and $(k - w_{2i+1})$ items belong to an increasing and a decreasing sub-sequences respectively, their contribution to ΔV can be reduced by moving $(k - w_{2i})$ leftward to the starting point of the increasing sub-sequence. Likewise, if the $(k - w_{2i+1})$ item belongs to an increasing sub-sequence while the $(k - w_{2i})$ item belongs to a decreasing sub-sequence, the contribution can be reduced by moving $(k - w_{2i+1})$ rightward to the ending point of the increasing sub-sequence (see two bold circles in Fig. 3). Since the starting and ending points of an increasing sub-sequence belong to the adjacent decreasing sub-sequences, each summing item in (9), $s((k - w_i)T + t_0)$, belongs to a decreasing sub-sequence in $Y^{(t_0)}$, in order to achieve the lower bound (minimum value) of ΔV. So, the summation ΔV is not less than the summation of $(V_{d\_\min,i} - V_{d\_\max,i})$, the contribution of two ending items of the decreasing sub-sequence. This means the bound (11) is the worst case. **End of Proof**.

To evaluate the '1' edge rising upper bound, instead we consider increasing sub-sequences in $Y^{(t_0)}$. We conclude with a similar theorem.

Theorem 3: The '1' edge rising upper bound for the worst case is:

$$y_{\max}(t_0 + kT) = \sum_{i=1}^{m} (V_{i\_\max,i} - V_{i\_\min,i}) + s(t_0), \qquad (12)$$

where m is the number of increasing sub-sequences in $Y^{(t_0)} = \{s(T + t_0), s(2T + t_0), \cdots, s(kT + t_0)\}$.

In Theorem 2 and 3, the value of k may be very large, even the infinite, to cover all decreasing or increasing stages in the step response waveform. Consequently, $Y^{(t_0)}$ becomes an infinite sequence and V_{sat} is the ending item of the last decreasing or increasing sub-sequence.

After identifying the decreasing sub-sequences in $Y^{(t_0)}$, the bit positions of signal transition making the lower bound is determined. With them, we can get the input stream $\{b_i, w_i\}$, and further the input bit pattern which causes the minimum '1' edge rising lower bound. The same thing applies to the maximum '1' edge rising upper bound. These two extreme values are denoted by $y_{\min}(t_0)$ and $y_{\max}(t_0)$, respectively. For a given t_0, we now can obtain $y_{\min}(t_0)$ and $y_{\max}(t_0)$, as well as the corresponding input bit patterns, by sweeping the sample points on step response. This is the basis for predicting the worst-case eye diagram and corresponding worst-case input bit patterns.

3.2 Worst-Case Timing Jitter

Due to the symmetry of eye diagram, the timing jitter is measured at the threshold voltage of $V_{sat}/2$. Because the voltage points $y(t_0 + kT)$ with different k's are superimposed at a same time position in the eye diagram, the jitter is determined by the earliest time of t_{J1} which makes $y_{\max}(t_{J1}) = V_{sat}/2$ and the latest time of t_{J2} which makes $y_{\min}(t_{J2}) = V_{sat}/2$ (see Fig. 4).

For a usual open eye, t_{J1} and t_{J2} exist around the t_{th} satisfying $s(t_{th}) = V_{sat}/2$, and their values are in the interval $(0, T)$. Furthermore, it is easy to prove that t_{J1} and t_{J2} have unique solutions, respectively. Otherwise, for example, if two different t_{J1}'s fulfilling $y_{\max}(t_{J1}) = V_{sat}/2$, a horizontal upper bound contour would appear in the eye diagram. This is impossible in a normal case. Therefore, with t_{J1} and t_{J2} fulfilling

$$y_{\max}(t_{J1}) = V_{sat}/2, \quad t_{J1} \in (0, T), \qquad (13)$$

$$y_{\min}(t_{J2}) = V_{sat}/2, \quad t_{J2} \in (0, T). \qquad (14)$$

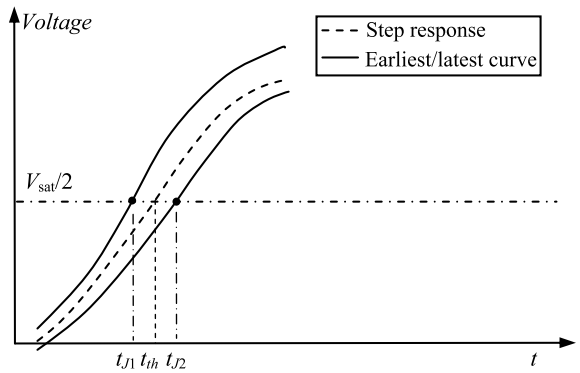


Fig. 4 Illustration of how to calculate the timing jitter.

We can calculate the jitter with:

$$t_{TJ} = t_{J2} - t_{J1}. \tag{15}$$

For a given step response, it is easy to find the t_{th}. With t_{th} and another time point forming the initial interval, a binary search algorithm can be used to solve (13) and (14), where functions $y_{\max}$ and $y_{\min}$ are evaluated with (12) and (11), respectively. When t_{J1} and t_{J2} are solved, the corresponding input bit patterns can also be obtained. Each time we evaluate $y_{\max}$ or $y_{\min}$, one sweep of step-response sample points is needed.

3.3 Worst-Case Eye-Opening Voltage

With Theorem 1, the eye-opening voltage can be calculated as the twice of the difference between the minimum rising voltage at a special time t_0 and $V_{sat}/2$. From Fig. 2, we see that when the maximum eye opening attained, the signal is experiencing "010" pattern and the signal just transits from one to zero. This means that the observing time $t_0 = T$ is for the maximum eye opening, as claimed in [2] and [4]. Therefore:

$$V_{EYE} = 2(y_{\min}(T) - V_{sat}/2) = 2y_{\min}(T) - V_{sat}. \tag{16}$$

With (11), we further have:

$$V_{EYE} = 2\left[s(T) + \sum_{i=1}^{m}(V_{d\_\min,i} - V_{d\_\max,i})\right] - V_{sat}, \tag{17}$$

where $s(T)$ is the step response at time T, and $V_{d\_\max,i}$ and $V_{d\_\min,i}$ are the maximal and minimal points on decreasing sub-sequences of $Y^{(T)}$.

Above deduction assumes that the maximum eye opening occurs with the '1' edge rising lower bound. However, the eye open may be contributed by a '1' edge holding lower bound (node 4 in Fig. 2) instead. The observing time is multiple T's larger than T. For example, if sequence $Y^{(0)} = \{s(iT)\}_{i=1}^{\infty}$ is a decreasing sequence, the minimum $y_{\min}(t_0) = V_{sat}$ when $t_0 = \infty$ accounts for the eye opening. In contrast, $y_{\min}(T) = s(T) - s(2T) + V_{sat}$ is larger than V_{sat}.

Evaluating the '1' edge holding lower bound involves checking t_0 beyond T. To unifying the operation and avoid checking different t_0's, we revise the definition of the sequence $Y^{(T)}$. We set the sequence starting from $s(T)$ instead of from $s(T + T)$. Once the initial $s(T)$ is included for finding the decreasing sub-sequences, the ΔV is able to derive the worst case for the '1' edge holding lower bound. This means we replace $Y^{(T)}$ with $Y^{(T)} = \{s(iT)\}_{i=1}^{\infty}$, and it is used for evaluating (17). In this way, if $s(T)$ is a starting point of a decreasing sub-sequence, the first difference term in (17) is able to replace $s(T)$ with a smaller value. With this extension, we are able to calculate the correct eye-opening voltage without modifying (17).

3.4 Algorithm Description and Analysis

Suppose the step response $s(t)$ of the system can be obtained by analytical formula or numerical algorithm. Or practically, $s(t)$ is just the transient simulation result of SPICE. In the latter case, a proper ending time for simulation is select so that the step response approaches to its saturated value. For transmission-line design, this ending time can be calculated with the line length and signal velocity. The saturation value V_{sat} can be calculated by solving the DC equation of the system. The algorithm for predicting the worst-case eye opening and jitter is as follows:

Algorithm Worst_eye (input: $s(t)$, V_{sat}, T, output: t_{TJ}, V_{EYE})
Find t_{th}, the time when step response crosses $V_{sat}/2$;
Use binary search to solve (13) and (14), where functions $y_{\max}$ and $y_{\min}$ are evaluated with (12) and (11), respectively;
Calculate t_{TJ} with (15);
Sweep the sequence $Y^{(T)} = \{s(iT)\}_{i=1}^{\infty}$, and then calculate V_{EYE} with (17).
End

We assume the number of sampled time points in the step response is n_s. We assume the time step is uniform and we should have an enough amount (T_N) of sample points in one symbol period for accuracy. Then in the proposed algorithm, the array size m_s for each observe time point t_0 is given by $m_s = \left\lceil \frac{n_s}{T_N} \right\rceil$.

The complexity of sweeping the sample points on step response to identify the local minimal and maximal is $O(m_s)$. The worst-case timing jitter applies binary search, so the complexity is $O(m_s \log n_s)$. The complexity for calculating worst-case eye opening is $O(m_s)$ because only one sweeping is needed.

There are two potential error sources for the proposed method. The first error source is the sampling time points. Because we only consider discrete sampling time points, inevitable error will be introduced. More sampling time points with smaller time step will achieve better accuracy with the cost of complexity. The other error source is the saturation voltage. The step response voltage will fluctuate in a very small range around saturation voltage after certain simulation time. It's hard to obtain the exact saturation voltage value. Also the effective voltage in the input bit pattern is

actually determined by the specific elapsed time. This small variation will introduce certain prediction error.

4. Validation of the Prediction Method

With an off-chip transmission line and two passive termination schemes, the accuracy and efficiency of the proposed prediction method is demonstrated.

4.1 Experiment Settings

A single-end transmission line is shown in Fig. 5. The line is on PCB with FR4 materials, connecting processors and memory. The line is 25 cm long, with frequency-dependent RLCG parameters extracted using a 2D EM solver called CZ2D from IBM [7]. The characteristic impedance is 50 Ω.

We assume the driver-side voltage source produces the input signal with 5 ps rise/fall time, and the V_{dd} is 1 V. Two termination schemes are applied. In the first scheme, both driver and receiver sides are connected with resistors. The second scheme is shown in Fig. 6, including a capacitor C_d and a resistor R_d at driver side. Due to the charging effect of C_d, the output voltage will rise rapidly when the step input switches to V_{dd} (see the middle curve in Fig. 1). Tuning the values of R_d and C_d may make the system's step response rising quickly and fluctuating little, so as to produce good eye diagram.

The proposed method is implemented with MATLAB, and the transient step response is simulated with IBM's PowerSPICE program [8]. In the experiments, we set the ending time of simulation 9 ns to obtain a saturated step response, because the wave reflection becomes negligible after two round trips for the lossy nature of the line. To facilitate evaluating $s(t)$, we fix the print time interval. All experiments are carried on a Linux workstation with 3.2 GHz Pentium 4 CPU.

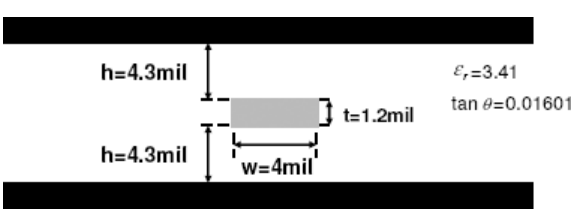


Fig. 5 The cross section of the single-end transmission line.

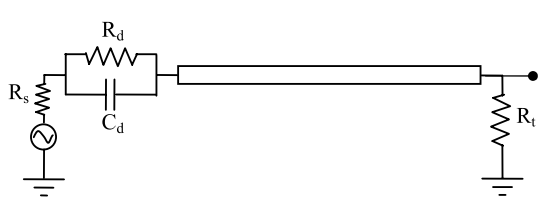


Fig. 6 The signaling scheme with driver-side capacitor.

4.2 Simulation Results

Since our method also generates the worst-case input bit pattern, taking it as input we can get the worst-case values of t_{TJ} and V_{EYE} through SPICE transient simulation. Different bit sequences lead to the earliest rising curve, the latest rising curve, and the '1' edge lower bound for eye opening. We concatenate them with sufficient non-transition bits. This worst-case input bit sequence usually includes several hundreds of bits. Here is an example:
{011111100000000000000000000001
111111111...(150 ones)
100000011111111111111111111101
111111111...(150 ones)
100000001111111111111111111101}.
This example includes, in turn, the bit sequences leading to the latest rising curve, the earliest rising curve, and the '1' edge lower bound for eye opening. And, the "150 ones" is the sufficient long separating bits.

For comparison, SPICE simulation with input of 2000-bit pseudo-random bit sequence (PRBS) is performed. This pseudo-random input is generated with a PRBS $2^{15} - 1$ data stream [9]. We also implemented the prediction method for V_{EYE} based on the assumption of bitonic step response [4]. Figure 7 shows the comparison of V_{EYE} and t_{TJ} obtained with different methods, for the first structure with resistance termination. Here we assume 10 Gbps signal and $R_s = 4\,\Omega$. From Fig. 7, we can see that the simulation results with the worst-case input pattern produce the bounds of eye-opening voltage and timing jitter. The results of proposed method match those from SPICE simulation with the worst-case input very well. The results from SPICE simulation with PRBS input and the prediction method in [4] have larger error. Compared with simulation results of the worst-case input, the error of simulation with 2000-bit PRBS is up to 40% on eye opening and 33% on jitter. The bitonic prediction also has 10% error on eye opening. The eye diagrams generated by SPICE simulation with the worst-case input and 2000-bit PRBS are given in Fig. 8, which shows the latter largely underestimates the worst case.

For the second structure with driver-side capacitor, we

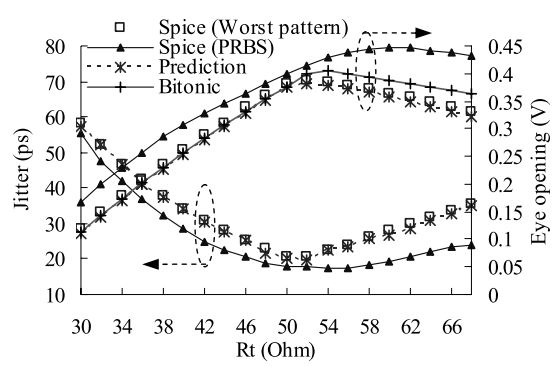
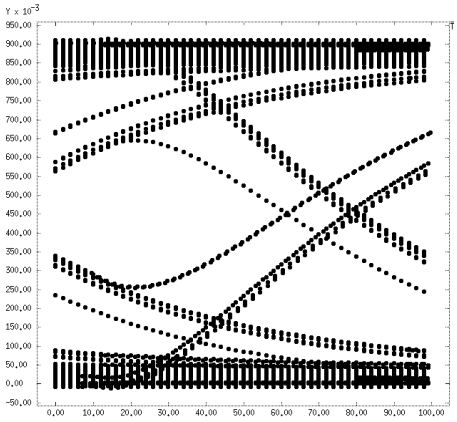
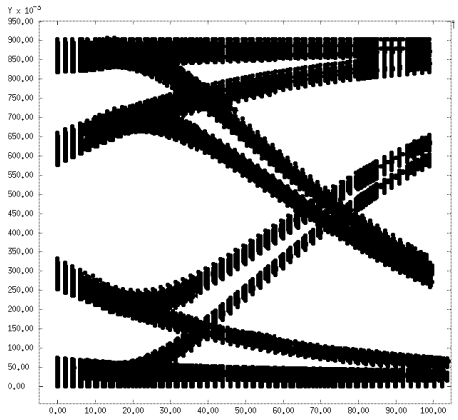


Fig. 7 Comparison of three methods on t_{TJ} and V_{EYE} for the resistive-termination scheme.



(a) SPICE result with the worst-case input



(b) SPICE result with 2000-bit PRBS

Fig. 8 Comparison of the eye diagrams for the resistive-termination scheme. ($R_s = 4\,\Omega$, $R_t = 52\,\Omega$, 10 Gbps)

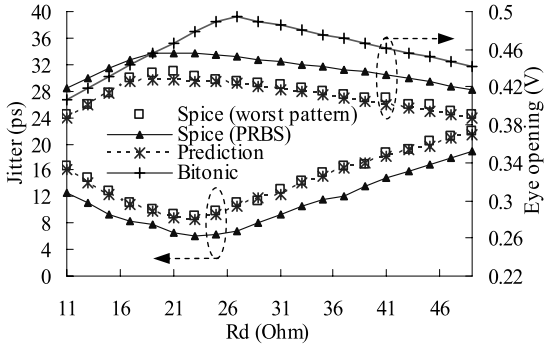
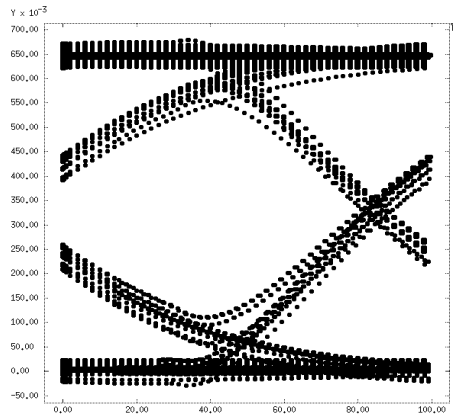
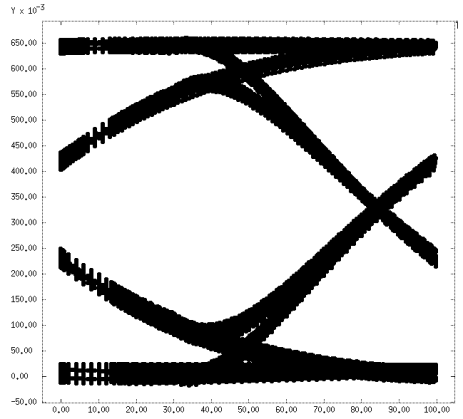


Fig. 9 Comparison of three methods on t_{TJ} and V_{EYE} for the series-capacitor scheme.

set $C_d = 4.5$ pF, $R_t = 55\,\Omega$, and change the value of R_d. Figure 9 shows the comparison of different methods on V_{EYE} and t_{TJ}. This figure validates the accuracy of our method again. The underestimation of SPICE simulation with PRBS input and the inaccuracy of method in [4] are also revealed. For this structure, the bitonic method behaves even worse than the SPICE simulation with PRBS, and it has the largest error of 16% on the eye opening. The reason should be the step response in the second structure is far from a bitonic



(a) SPICE result with the worst-case input



(b) SPICE result with 2000-bit PRBS

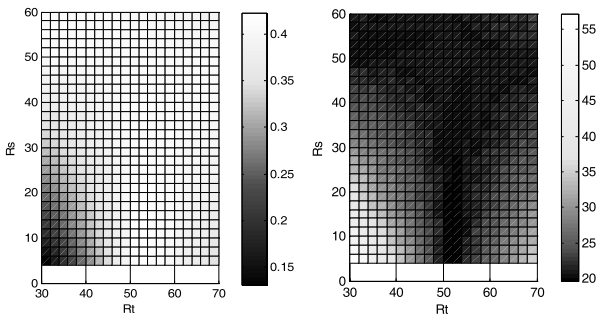
Fig. 10 Comparison of the eye diagrams for the series-capacitor scheme. ($C_d = 4.5$ pF, $R_d = 23\,\Omega$, $R_t = 55\,\Omega$, 10 Gbps)

waveform. The eye diagrams generated by SPICE simulation with the worst-case input and 2000-bit PRBS are compared in Fig. 10.

For a typical case, the total CPU time of proposed method is 5.55 s, including 3.43 s spent on SPICE simulation for the step response. In the rest time, 2.06 s is spent for reading in the step response, while the time for the predicting algorithm is less than 0.1 s. The corresponding CPU time of SPICE simulation with 2000-bit PRBS is 78.20 s. Our method is several ten times faster than the simulation method with 2000 bits, while producing accurate results. We have also done experiments with longer PRBS input up to 20000 bits, which reveal that the error on eye opening or jitter is still larger than 15%. This suggests that the simulation method with PRBS input is not feasible for predicting the worst-case eye diagram.

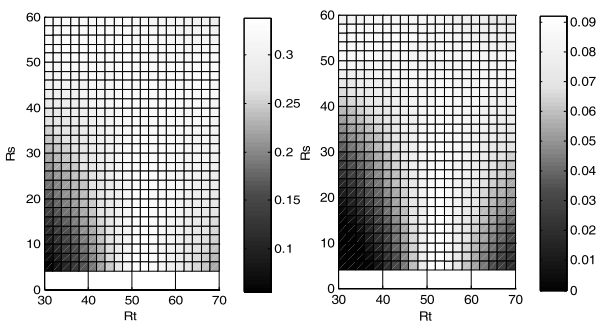
5. Application to Low-Power Equalizer Design

With a fixed signal rise/fall time, the proposed method takes only one step response to predict the worst-case eye diagram for different signaling bit rates. So, the proposed method is very efficient to evaluate the signaling quality under different design conditions. The two termination schemes in



(a) V_{EYE}/V_{sat} (b) t_{TJ} (in unit of ps)

Fig. 11 Normalized eye-opening and jitter for various R_s, R_t. (data rate is 10 Gbps)



(a) 10Gbps (b) 13.3Gbps

Fig. 12 Normalized eye-opening area A_{EYE}, for various R_s, R_t.

Sect. 4.1 provide low-power equalizers to the off-chip transmission line. With the help of proposed method, we search the optimal parameters for the passive equalizers. Besides t_{TJ} and V_{EYE}, a metric standing for the normalized eye open area:

$$A_{EYE} = AREA_{EYE} \cdot 2/(T \cdot V_{sat}), \tag{18}$$

is used for evaluating the signaling quality.

5.1 Scheme with Only Resistive Termination

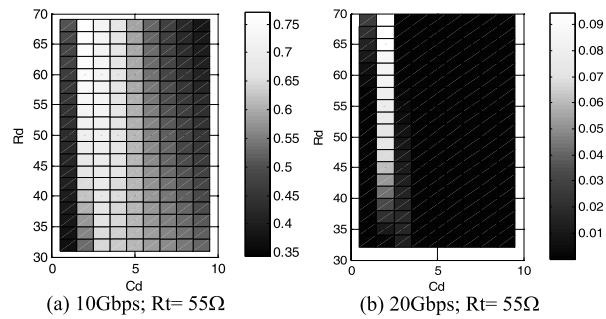
In the experiments, R_s varies from 4 Ω to 70 Ω, and R_t varies from 10 Ω to 70 Ω, both with step size of 2 Ω. Utilizing the proposed method, we evaluate t_{TJ}, V_{EYE}, and A_{EYE} for signaling speed of 10 Gbps, 13.3 Gbps and 20 Gbps. To correctly reflect the signal quality, the normalized eye-opening (V_{EYE}/V_{sat}) and jitter at 10 Gbps are plotted in Fig. 11, including the optimal results. The optimal eye opening is achieved when R_s = 4 Ω and R_t = 52 Ω, with V_{EYE}/V_{sat} = 0.42. The optimal jitter is 19.7 ps, when R_s = 20 Ω and R_t = 50 Ω. The results of A_{EYE} at 10 Gbps and 13.3 Gbps are shown in Fig. 12. For signal throughput beyond 13.3 Gbps, i.e. with clock period less than 75 ps, our method predicts that there is no eye opening at all. From the figures, we can see that impedance matching at the receiver side seems more important than matching at the driver side.

The predicted maximum normalized eye area for different bit rates are listed in Table 1, with corresponding resistance values and the estimated jitter and eye-opening voltage. The average dynamic power P is also provided in Table 1, which is obtained from the SPICE simulation with PRBS input. For the optimal structure under 10 Gbps, the eye diagrams generated by SPICE simulation with the worst-case input and 2000-bit PRBS are shown in Fig. 8. For this scheme with only resistive termination, the eye is closed when signaling speed increases to 20 Gbps.

Table 1 Optimal A_{EYE} and other metrics for the first scheme.

	R_t (Ω)	R_s (Ω)	A_{EYE}	t_{TJ} (ps)	V_{EYE} (V)	P (mW)
10G	52	4	0.339	19.9	0.381	8.85
*10G	52	40	0.327	20.5	0.228	5.18
13.3G	52	4	0.092	30.4	0.140	8.85
*13.3G	52	36	0.088	31.1	0.087	5.33

*The row includes the practical parameter choice considering variation, and the corresponding eye diagram metrics.



(a) 10Gbps; Rt= 55Ω (b) 20Gbps; Rt= 55Ω

Fig. 13 Normalized eye-opening area A_{EYE}, for various R_d, C_d.

Although A_{EYE} attains the optimal value when R_s = 4 Ω, it is observed from Fig. 11 and Fig. 12 (especially Fig. 11(b)) that the eye quality becomes very sensitive to variation of R_t if R_s = 4 Ω. Considering the resistance variation may be larger than 10%, we shall choose larger R_s to make the eye quality less sensitive to R_t. Based on this observation, two rows are inserted in Table 1 to show the examples of practical parameter choice and the corresponding eye diagram metrics.

5.2 Scheme with Driver-Side Series Capacitor

In the second scheme, a small driver with input impedance R_s = 5 Ω is assumed. We try R_t with values of 45 Ω, 50 Ω, 55 Ω and 60 Ω, to avoid severe impedance mismatching. At the driver side, R_d varies from 1 Ω to 70 Ω with step size of 1 Ω, and C_d varies from 0.5 pF to 20 pF with step size of 1 pF. The proposed method predicts that there is eye open even when signal throughput increases to 20 Gbps. Some results of A_{EYE} are shown in Fig. 13. The predicted maximum A_{EYE} and corresponding R, C values, and other performance metrics are listed in Table 2.

From Table 1 and Table 2, the advantage of the series-capacitor scheme can be observed. For 10 Gbps signal transmission, the normalized eye area in the second scheme is 2× larger that in the first scheme. While for 13.3 Gbps signal, the advantage on eye area increases to 5×. For higher signal throughput which the first scheme cannot afford, the

Table 2 Optimal A_{EYE} and other metrics for the second scheme.

	$R_t(\Omega)$	C_d(pF)	$R_d(\Omega)$	A_{EYE}	t_{TJ} (ps)	V_{EYE}(V)	P(mW)
10G	55	1.5	65	0.768	12.5	0.375	4.76
13.3G	60	1.5	66	0.494	12.5	0.268	4.73
20G	55	1.5	64	0.095	20.1	0.069	5.00

second scheme still works. From Table 1 and Table 2, we see that the power consumption of both schemes mainly depends on the resistance elements involved, and the scheme with driver-side series capacitor does not increase the power consumption.

6. Conclusions

An efficient and accurate method is developed to analyze the signal distortion from inter-symbol interference. This method utilizes the step response of the signaling system to extract the worst-case eye diagram, including the eye opening and timing jitter. It also generates the input data patterns causing the worst-case inter-symbol interference. Experimental results demonstrate the accuracy and efficiency of the proposed method. The proposed general-purpose method is very useful to analyze various high-speed signaling systems.

The proposed method is applied to design space exploration for passive equalizer schemes of off-chip transmission line. Simulation results show that a scheme with driver-side series capacitor remarkably improves the signal quality compared with the conventional resistance termination scheme, while not increasing the power.

The peak distortion analysis [1] based on the unit pulse response is only applicable to digital signals with symmetric rise/fall time. On the contrary, the proposed method can be easily extended to handle signals with asymmetric rise/fall time if using two step responses. It can also be utilized in circuit design applications considering noise margin. These issues could be explored in the future.

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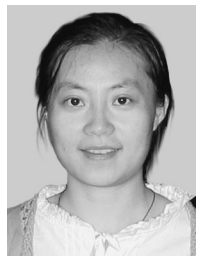

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