A 3-D Parasitic Extraction Flow for the Modeling and Timing Analysis of FinFET Structures

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***Abstract*—The FinFET technology is considered as the best candidate to extend the CMOS technology down to 10 nm. In this paper, a three-dimensional (3-D) parasitic extraction flow is proposed for modeling and timing analysis of the FinFET based circuits. The flow fully considers the 3-D geometry of the FinFET and employs accurate field solvers for extracting resistances and capacitances. Thus, it accurately captures the prominent coupling effect between the FinFET and lower-layer interconnects. With the input of industry-standard layout data, the flow outputs the SPICE RC netlist for timing analysis. Numerical experiments on FinFET structures and other digital design demonstrate the efficiency and accuracy of the proposed extraction flow. This work provides an efficient supplement to the exiting parasitic extraction methodology for the FinFET technology.**

I. Introduction

As the feature size continues decreasing, the scaling of the traditional planar MOSFET becomes more and more difficult due to small geometry effects, e.g., short channel effect, drain-induced barrier lowering. This has promoted the development of the new device architecture in which multiple gates are used per device, which is known as multi-gate devices. Among them, FinFET (Fin Field Effect Transistor) is the most promising one for its ease to be manufactured [1-2]. The new transistor has higher scalability than the traditional counterparts since more than one gate can be used to control the potential of the channel. Despite the advantage of scalability of FinFET, the parasitic effect in FinFET is more prominent than the traditional counterpart due to the non-planar structure. The coupling capacitance between the fin-shaped channel extension and other parts of the circuit is much larger than that in the planar MOSFET. The resistance of the narrow long channel extension is also larger than the traditional one for its small area of cross section. Therefore, more accurate methodology of parasitic extraction is required for the modeling and simulation of the integrated circuit with FinFET devices.

In the device of FinFET, the source and drain are connected with a long and thin fin-shaped channel. The channel is wrapped from three sides by the gate. The channel is un-doped or lightly doped, and there are often high-k dielectric between the channel and gate to enhance the controllability of channel and reduce the leakage current. The diffusion area in source and drain are enlarged so that it is easier to contact via with source/drain diffusion while reducing the contact resistance [1]. To demonstrate the structure of FinFET, we show a single fin structure of a SOI FinFET in Fig. 1.

Previous works have considered three kinds of parasitic parameters in the FinFET: source/drain series resistance, gate resistance, and gate capacitance [2]. Some of them are devoted to the modeling of the three parasitic parameters, where several analytical models were proposed [3-6]. While some of them has simulated the performance of the design based on FinFET [10], however, most of the works treated interconnects and FinFET device as two separated system, few of them have considered the coupling effect between FinFET and the interconnects. As can be observed from Fig. 1, the cross section of fin is small and the length of it is relevant long. So, the resistance from source to drain is larger than the traditional MOSFET. Due to the nature of 3-D geometry of FinFET, the coupling effects between fins and gate are very prominent. However, few of existing works have considered the coupling effect between the 3-D FinFET and interconnect metal wires. In this work, a parasitic

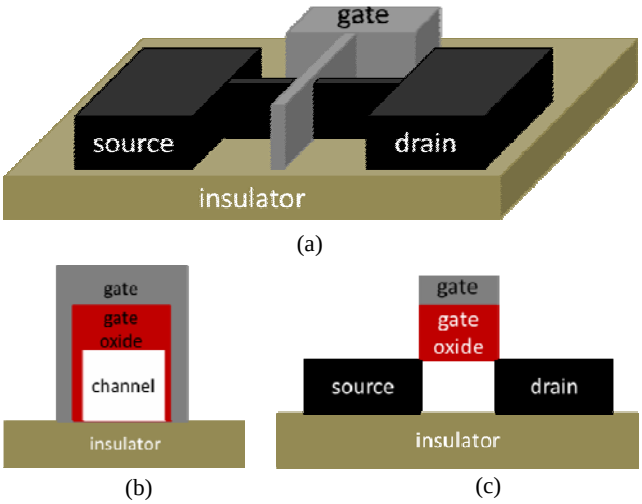

Fig. 1 (a) The 3-D view of the structure of a single fin SOI FinFET (b) the cross section view of the channel, and (c) the cross section view along the channel.

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extraction flow for 3-D FinFET is presented, which takes in the GDS layout data and outputs the RC netlists. Unlike StarRC, the industrial golden value of 2-D device simulation, which employs the method of pattern matching to extract the coupling effect, the proposed flow of us employs 3-D field solvers to extract the resistances and capacitances of FinFET design, which is able to accurately capture the coupling effect between the FinFET and lower-layer interconnects. The techniques of metal segmentation and capacitance distribution are implemented to produce distributed RC elements, which ensure an accurate timing analysis. Numerical experiments on a single fin structure validate the 3-D extraction flow, and show the prominent coupling effect between the gate of FinFET and the M2 interconnects. A design of 2-bit adder is also extracted, which demonstrates the efficiency of the proposed extraction flow. In the experiments, the HSPICE is also used to report the propagation delay of nets in FinFET and signal interconnects.

This paper is organized as follows. The background of the extraction flow is described in Section II. The detailed description of each step of the flow is given in Section III. In Section IV, we demonstrate some numerical results. Finally, the conclusions are drawn in Section V.

II. The 3-D Extraction Flow for FinFET Modeling

To simulate the behavior of FinFET based design, accurate extraction of parasitic resistance and capacitance is a must. We propose a flow for the extraction of parasitic parameters and timing analysis, considering the structures of FinFET. The flow chart of the proposed flow is shown in Fig. 2. The data of circuit layout is in the format of GDS (graphic database system), which can be obtained from any physical design tool. The final output of the flow is the propagation delay considering the influence of parasitic RC of FinFETs.

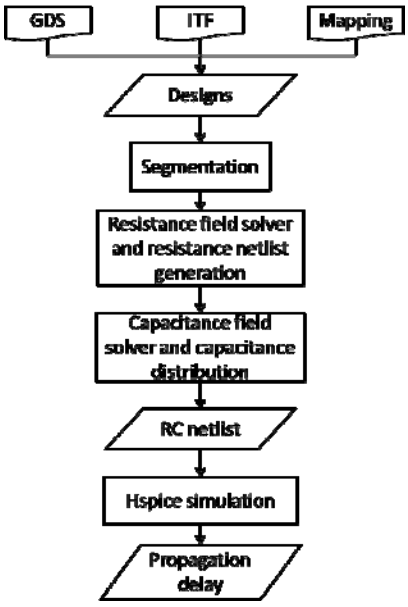

Fig. 2 The flowchart of the proposed extraction and simulation flow.

The GDS file only contains the 2-D layout information on specific layers. To accurately describe 3-D geometry, the information about all layers is required. For this purpose, we use the ITF (Interconnect Technology Format) file to describe the layer information. However, the layer names in the GDS file is not always the same with the names used in ITF file. Therefore, another mapping file is needed. With the three input files, 3-D geometry objects can be constructed for the FinFETs and adjacent metal wires.

Another important task is to segment the conductor objects into small and relevant regular shapes. This guarantees the accuracy of modeling and lowering the computational burden. The algorithm of sweeping line is adopted in the stage of segmentation.

After the segmentation, the physical objects of layout should be converted to a symbolized circuit netlist, for the purpose of modeling and simulation. The field solvers for resistance extraction and capacitance extraction are used to guarantee the accuracy, whose results are used to form the netlist. Since the coupling capacitances are between physical nets, the step of distributing the capacitances to the circuit nodes is an importance task. After all the previous steps, the parasitic RC netlist is generated. And then, we can add waveform to the pins and test the propagation delay of the specific nets.

III. Technical Details of Extraction and Netlist Generation

A. The input data for FinFET modeling

In the GDS formatted layout data, the information of interconnects and devices, including names, shapes and coordinates in the XOY plane, is given. To obtain the coordinates in the Z direction, we use ITF file as another input. Another mapping file is needed to match the names in the GDS file and ITF file together. The ITF file contains the information of the process cross section and connectivity of layers. It describes the thickness and physical attributes of the conductor and dielectric layers. An example of the technology with FinFET devices is shown in Fig. 3.

B. Segmentation and connectivity extraction

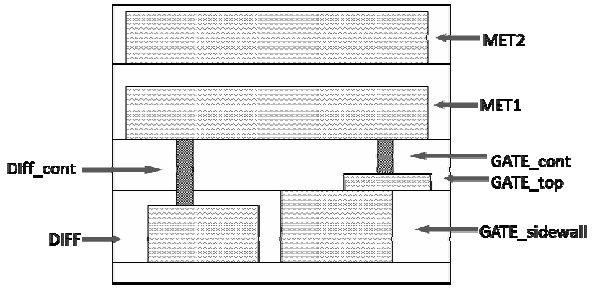

Fig. 3 An example of technology described in ITF, for the design of FinFET based circuit.

The task of segmentation is to divide a large net into a set of small nets, which are the minimum unit of RC extraction in our flow. So the segmentation directly influences the accuracy and computational speed of the simulation flow. If the segmentation is too coarser, the modeled netlist is not accuracy enough to model the real case and the distribution of coupling capacitance is hard to be accuracy; on the other hand, if the segmentation is too fine, the time cost is not acceptable. To maintain the balance, our segmentation procedure is divided into two steps: a) segment the polygons into rectangles, b) segment the rectangles with high length-width ratio into smaller ones. The flow of segmentation is demonstrated in Fig. 4.

The connectivity extraction is to construct the connectivity undirected graph for each net. This step is for generating the RC netlist for simulation.

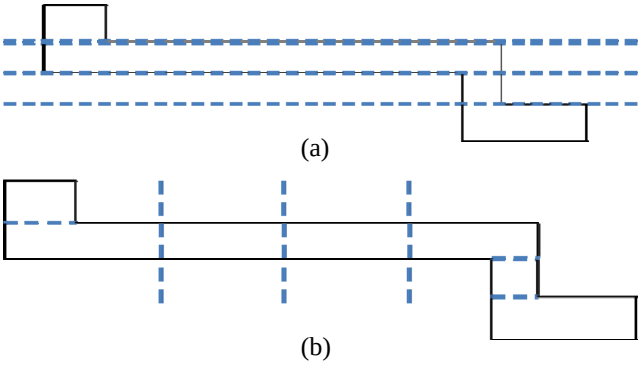

Fig. 4 The polygon segmentation strategy. (a) the sweep procedure (b) the procedure to segment the rectangles with high length-width ratios.

C. *Resistance extraction and netlist generation*

For each conductor segment, the resistance needs to be extracted. 3-D field solver is employed to achieve the best of accuracy. However, this may consumes a lot of computational time. In our work, the square-counting approach is also used for some rectangular segment. This keeps the same accuracy while reducing the total computation greatly. For the 3-D segments demanding field solver, we needs to specify the ports explicitly. The potential on each port is assumed to be identical. The field solver will generate a resistance matrix connect all the ports together, i.e., if there are n ports, an equivalent resistance network with n×n resistors will be generated. In this work, the connecting surface of adjacent segment is assumed to be the port for resistance extraction. Corresponding to each port, a node is generated into the resulting circuit. Fig. 5 shows an example of generating the resistance network from conductor structure.

D. *Capacitance extraction and distribution*

For the capacitance extraction with 3-D accuracy, the whole structure should be simulated by the field solver. Therefore, the efficiency and capability is the major concern for choosing the solver. During the past two decades, a lot of

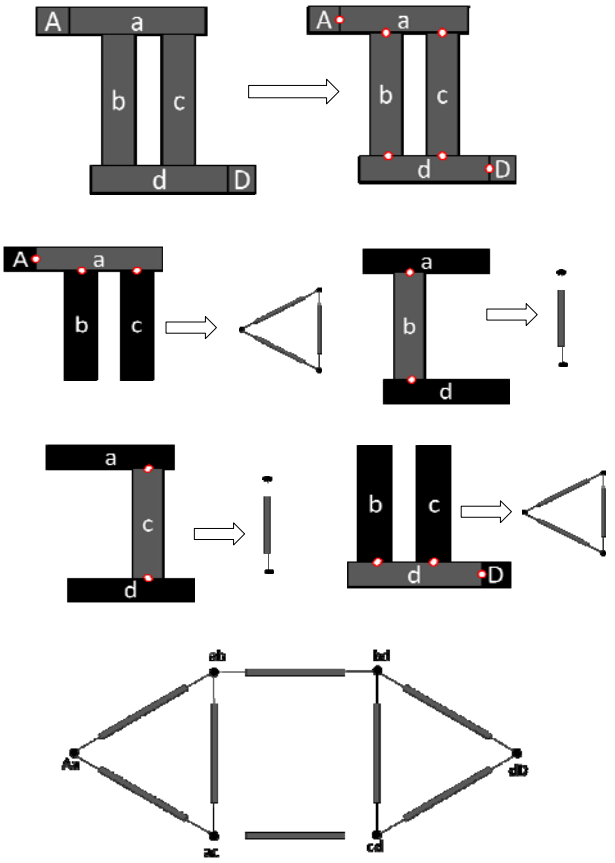

Fig. 5 A 2-D structure of conductors for the illustration of the netlist generation. (a) The structure with nodes generated according to connectivity analysis. (b) Four portions of the structure and their corresponding resistance circuits. (c) The overall equivalent resistance network for (a).

fast approaches to extract the capacitance for large scale interconnects have been proposed. Among them, the most famous methods are boundary element method (BEM) [11] and floating random walk algorithm (FRW) [9]. For the large scale problem, FRW outperforms BEM both in simulation time and memory. For this reason, we use the capacitance solver employing the floating random walk algorithm in this work. It has the advantages of lower memory usage, more scalability for large structures, and better parallelism. In the floating random walk algorithm, walks start on the Gaussian surface randomly, and the final convergence criterion assures that the error of capacitance on the large net group is smaller than a threshold.

Because the floating random walk solver extracts the capacitances of nets, we need to distribute the capacitance to the nodes connecting them. To account for the non-symmetry of structure, we adopt a strategy that distributes the capacitance of a net to its nodes according to the weight of surface area near the node. Finally, a distributed RC netlist is generated for the ease of timing simulation.

IV. Numerical Results

In this section, we present some numerical results

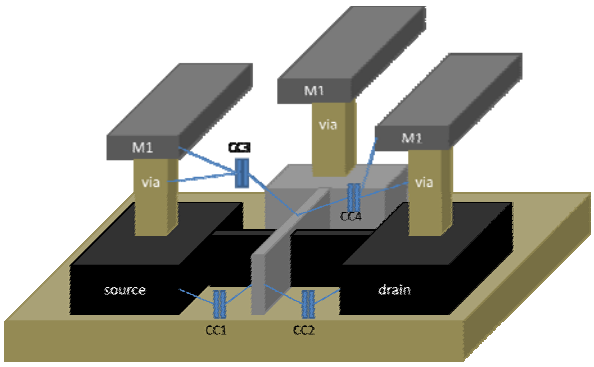

Fig. 6 The simulated structure and the components of gate parasitic capacitance, where cc1 and cc2 and the coupling components with device, cc3 and cc4 and the coupling components with interconnects

regarding the 3-D extraction flow. The whole extraction flow is implemented in C++. The 3-D capacitance solver used is a commercial floating-random-walk solver, called Rapid3D [7]. For 3-D resistance extraction, the Raphael rc3 [8] which is based on finite difference method is used. The timing results are obtained with the HSPICE. All experiments are carried out on a Linux server with 2.67GHz.

A. *A FinFET structure*

Different with traditional planar devices, the coupling effects between devices and interconnects are more notable for FinFET because of its 3-D geometry. As a result, when simulating the propagation delay in the device, it is important to take the lower-layer interconnects into account. The structure we used to simulate contains the device of FinFET, routings of M1 layer and the vias connected M1 to device. The 3-D view of the structure is shown in Fig. 6. The geometric parameters of the structure are listed in Table I.

TABLE I. THE GEOMETRIC PARAMETERS OF THE FINFET STRUCTURE

Parameter	Description	Value
L_g	Physical Gate Length	50nm
H_{fin}	Fin Height	100nm
W_{fin}	Fin Width	20nm
L_{ext}	Source/Drain Extension Length	100nm
T_{poly}	Poly Thickness	10nm
T_{ox}	Thickness of Gate Oxide	1.3nm

By simulating the structure with field solver, we obtain the coupling capacitances of gate with other components, as listed in Table II. From the table we can see that the coupling between the gate and M1 interconnect is comparable to the coupling between the gate and source/drain. For this structure, the total computational time of our flow is about 30 seconds, which validates its efficiency.

TABLE II. THE COUPLING CAPACITANCE OF GATE WITH OTHER COMPONENTS OF THE FINFET STRUCTURE

Capacitance	Description	Value (F)
cc1	The coupling between gate and source	1.98E-17
cc2	The coupling between gate and drain	1.84E-17
cc3 + cc4	The coupling between gate and the interconnect with source and drain	1.25E-17

We then simulate the signal propagation from M1 layer to the channel through the nets of source, drain and gate, respectively. The whole design is segmented into 16 small nets, which results in a netlist with 16 nodes. With the extracted RC netlist, the propagation delays are simulated with HSPICE, which are listed in Table III.

TABLE III. THE PROPAGATION DELAY OF EVERY NET GROUP

Net group	Propagation delay (s)
Drain	3.786E-13
Gate	7.577E-14
Drain	3.307E-13

B. *A 2-bit adder design*

Since the comparison with other 3-D extraction tool for the FinFET modeling is not available, we use a 2-bit adder design circuit based on 2-D MOSFET to partially verify the accuracy of our extraction flow. Our flow occupies 3-D field solver to simulate the capacitance and resistance, as the result, the validness for 2-D flow can suggest the validness for the 3-D FinFET design.

The bird eye view of the structure of 2-bit adder is shown in Fig. 7. Our results are compared with those extracted with StarRC, which is regarded as the golden tool for such digital design.

The 2-bit adder contains 9 electronic isolated net groups. The conductors are segmented into 90 nets and generated 82 nodes to symbolize the design. The comparisons of the

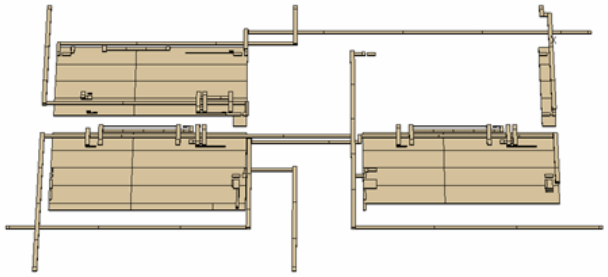

Fig. 7 Bird eye view of the structure of the 2-bit adder.

capacitance of our flow and StarRC are listed in Table IV. The results show that the discrepancy is always below 10%, and mostly below 5%. The total computational time of our flow is about 220 seconds, for this design.

TABLE IV. THE COMPARISON OF THE TOTAL CAPACITANCE OF EACH NET GROUP BETWEEN STARRC AND OUR FLOW

Net group	StarRC capacitance (F)	Our flow capacitance (F)	Relative error
SUM1	2.20575E-14	2.24154E-14	1.62%
SUM0	1.6737E-14	1.59854E-14	-4.49%
COUT	3.56454E-14	3.64919E-14	2.37%
C	1.9558E-14	2.09678E-14	7.21%
B1	7.18069E-15	7.82822E-15	9.02%
B0	2.2605E-14	2.31368E-14	2.35%
A1	4.41075E-14	4.314E-14	-2.19%
A0	8.38196E-15	8.59976E-15	2.60%

We then do timing analysis with both the netlists obtained by StarRC and our extraction flow. If listed in order of the propagation delay, we find the same critical nets with the both results. In Table 5, we give the data of the first three nets with larger delay, which shows the discrepancy from both netlists is small.

TABLE V. THE PROPAGATION DELAY COMPARISON OF OUR FLOW AND STARRC FOR THE CASE OF 2-BIT ADDER

Pair #	StarRC delay (s)	Our flow delay (s)	Relative error
2	3.51E-13	3.77E-13	7%
6	2.71E-13	2.23E-13	-17%
8	1.12E-13	1.17E-13	5%

V. CONCLUSIONS

Fin and multi-fin field effect transistors are supposed to be the next generation device to take over the baton from MOSFET to continue the Moore's law. Despite the advantage of FinFET, the RC parasitics caused by the non-planar property has eroded the advantage of scaling. Thus, accurate modeling of the parasitics of FinFET based design is an extremely important task. The traditional RC extraction tool cannot support the design of FinFET well and the existing research does not pay enough attention to the coupling effect between the device and the metal interconnects. In this paper, we propose a 3-D extraction flow for modeling the RC parasitics in FinFET structure, and further for the timing analysis. The 3-D field solvers are integrated into this flow, and it has been demonstrated to be efficient and accurate. The presented flow makes a seamless connection with the traditional layout parasitic extraction flow.

In the future work, the parallel computing and better segmentation technique for multi-fin FinFET modeling will be considered to improve the efficiency and versatility of the presented flow.

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