Random Walk Based Capacitance Extraction for 3D ICs with Cylindrical Inter-Tier-Vias

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***Abstract*—Three-dimensional integrated circuits (3D ICs) make use of the vertical dimension for smaller footprint, higher speed, lower power consumption, and better timing performance. In 3D ICs, the inter-tier-via (ITV) is a critical enabling technique because it forms vertical signal and power paths. Accordingly, it is imperative to accurately and efficiently extract the electrostatic capacitances of ITVs using field solvers. Unfortunately, the cylindrical via shape presents major challenges to most of the existing methods. To address this issue, we develop a novel floating random walk (FRW) method by rotating the transition cube to suit the cylindrical surface and devising a special space management technique. Experiments on typical ITV structures suggest that the proposed techniques can accelerate the existing FRW and boundary element method (BEM) based algorithms by up to 20X and 180X, respectively, without loss of accuracy. In addition, compared with the naïve square approximation approach, our techniques can reduce the error by 10X. Large and multi-dielectric structures have been tested to demonstrate the versatility of the proposed techniques.**

Keywords—capacitance extraction; floating random walk method; monolithic inter-tier via (MIV); three-dimensional (3D) IC; through-silicon-via (TSV)

I. INTRODUCTION

Three-dimensional integrated circuits (3D ICs) are generally considered to be one of the most promising solutions that offer a path beyond Moore's law. By integrating multiple tiers vertically, 3D ICs provide smaller footprint, higher speed, lower power consumption, and better timing performance. There are in general two types of 3D ICs: die stacking and monolithic integration. Die stacking based 3D ICs simply stack multiple two-dimensional dies fabricated through conventional processes using through-silicon-vias (TSVs) [1-4]. It is fully compatible with existing processes, but the TSVs are large in size to ensure proper wafer handling and alignment. On the other hand, monolithic integration uses monolithic inter-tier vias (MIVs) to connect multiple device layers fabricated sequentially. It requires innovative fabrication process [5-7], but allows the MIV to be much smaller than the TSV. In this paper, we use inter-tier-via (ITV) to denote both the TSV and the MIV.

ITVs play a critical role in 3D ICs to deliver signal and power vertically, and therefore their parasitics need to be accurately modeled. High-precision parasitic extraction for ITVs has become a key challenge due to the rising number of 3D analog effects, narrowed performance margins and time windows. Overestimation of ITV parasitics results in excessive guardbands, which impacts performance and degrades the benefits of the 3D technology. On the other hand, underestimation of parasitics causes potential timing failures and yield loss.

Among the parasitics, the ITV coupling capacitance has attracted much attention, due to its large impact on timing and noise analysis. Most existing works focused on the ITV's electrical model and the extraction of its cylindrical metal-oxide-semiconductor (MOS) capacitance [1-3]. Few works were devoted to the electrostatic coupling capacitances among ITVs and horizontal wires, especially in the context of general layout structures. In [4], a set of analytical formulas were proposed for the coupling capacitance among ITVs and wires. It was also revealed there, that the electrostatic capacitance can be comparable to the MOS capacitance, and should not be ignored. However, the technique was derived from the square-shape assumption of TSV, which obviously differs from the reality and may have large error. And, the analytical technique is only applicable to regular TSV placements, whereas its error for random TSV placement was shown to reach 20% [4].

A more comprehensive approach to capture the parasitic capacitance of ITVs is to use field solvers [8-15]. Field solvers for capacitance extraction are mainly attributed to two categories: the boundary element method (BEM) [13-15] and floating random walk (FRW) method [9-10, 12]. Generally speaking, BEM runs faster than the FRW method for small- and medium-size problems. Yet its accuracy largely depends on the quality of boundary discretization and is therefore not very stable. On the other hand, FRW method is a discretization-free method, and thus enjoys the advantages of better scalability for large structures, tunable accuracy, and higher parallelism, etc. Unfortunately, none of these methods apply to the ITV capacitance extraction directly, mainly due to the cylindrical shape of ITV.

If we employ BEM, we shall first use a polyhedron to well approximate the cylinder shape. This may cause a dense panel discretization. Taking into account the large dimensions of ITV, we can anticipate that such approximation can induce a large number of unknowns and large computational cost. On the other hand, the existing FRW algorithms for capacitance extraction assume that the considered geometries are all

This work was supported in part by NSFC (No. 61076034), the Beijing Natural Science Foundation (No. 4132047), the Tsinghua University Initiative Scientific Research Program, and the Opening Foundation of ASIC and System State Key Laboratory (Fudan University, No. 12KF009).

rectilinear-shaped [9-10, 12]. This limits their application only to the Manhattan geometries of interconnect wires in digital circuits. One naïve solution is to approximate the cylindrical ITV with square-shape objects, but as we will demonstrate in the experiments, the approximation causes large error.

In this work, we propose a novel method for ITV parasitic capacitance extraction considering its cylindrical shape. We first evaluate the error brought by the square approximation of cylinder with several typical ITV structures. Then, based on the FRW algorithm, an approach with rotated transition cubes is proposed to accurately model the cylindrical ITVs. A special space management technique is also devised to efficiently handle general large-scale structures in 3D ICs. Numerical experiments validate the accuracy of the proposed techniques, which show that we can reduce the error caused by the square-approximation approach by more than 10X with affordable runtime overhead. Compared with the BEM solvers [13, 14], the proposed FRW based method also exhibits several tens times speedup and huge memory save, while guaranteeing stable accuracy. In addition, experiments have been carried out to show the scalability of the proposed method to large structures and its feasibility to actual multi-dielectric structures.

The main contributions of this work are as follows:

1) To the best of the authors' knowledge, this is the first field solver that can directly handle cylindrical ITVs without any geometric approximation. Experiments have verified the high accuracy of the proposed method.
2) It is also the first work handling non-Manhattan geometries with the random walk method using cubic transition domains.
3) By utilizing the rotated transition cube and special space management techniques, the proposed method inherits the advantages of the FRW algorithm for capacitance extraction. Its speedup over a simple extension of original FRW method is up to 20X. It is also more than 10X faster than fast BEM algorithms, while accurately calculating total and coupling capacitances and greatly saving the memory cost.

II. Preliminaries

A. Modeling of ITVs in 3D ICs

There are in general two types of 3D ICs: die stacking with TSVs and monolithic integration with MIVs. The die stacking based 3D ICs can be further divided into different types such as face-to-face, face-to-back, etc. The TSVs are mainly fabricated with three technologies: TSV-first, TSV-middle and TSV-last. Under the TSV-first technology, devices and TSVs are fabricated first, and then metal layers are deposited. So, TSVs are surrounded by other TSVs laterally, and by wires mostly vertically [see Fig. 1(a)]. With the TSV-last technology, TSVs are fabricated after metal deposition, which makes them go through all the layers from the substrate to the topmost metal layer. Therefore, TSVs are surrounded by other TSVs laterally and by interconnect wires laterally and vertically [see Fig. 1(b)]. Due to some fabrication issue, the size of TSV is much larger than that of conventional via. It is of cylinder shape, with diameter larger than 1 μm (typically 5 μm). Going through the entire substrate, the TSV usually has a large aspect ratio (height/diameter, typically 10).

In Fig. 1, we show the capacitive couplings among TSVs and wires. C_{TT} and C_{TD} are the capacitances between two TSVs,

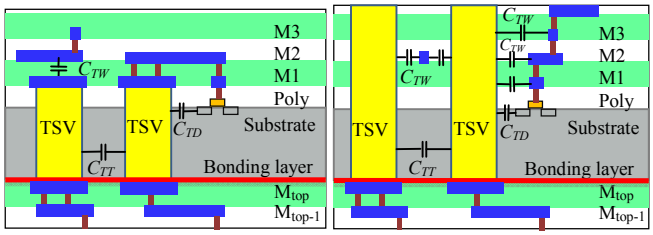

Fig. 1. Cross-section views of the TSV-first technology (a), and TSV-last technology (b) for the parallel 3D IC.

and between TSV and device, respectively. They involve the semiconductor effects in silicon substrate. In previous works, e.g. [1-4], the circuit model to capture the coupling among TSVs has been proposed. All of them, except [4], paid attention to the calculation of the MOS capacitance component in C_{TT} and C_{TD}, rather than the electrostatic capacitance component and C_{TW} shown in Fig. 1. In [4], an analytical approach was proposed to approximately calculate the electrostatic capacitances of TSVs, whose results showed that the electrostatic capacitance (~32.2fF excluding TSV-to-wire coupling) could be as large as half of C_{MOS} (~68.8fF).

The topology of MIVs and wires in monolithic 3D IC is similar to that of TSVs and wires shown in Fig. 1. The difference is that MIVs have much smaller size and much larger density as well [5-6]. The diameter of MIV is similar to that of local via. However, since MIV passes through the device layer and inter-layer dielectric (ILD), it has larger aspect ratio. Therefore, it is more important to accurately extract the MIV's capacitance than that of local via (sometimes ignored).

To sum up, we find out that accurately calculating the electrostatic capacitances of TSV/MIV in 3D IC is important, and very few works have considered it. Furthermore, no one considers the 3D cylinder shape of these inter-tier-vias (ITVs) while calculating electrostatic capacitances. To evaluate the effect of the square approximation [4] on the extracted ITV capacitances, we have simulated three typical TSV and MIV structures, as listed in Table I. The TSV-first structure is a "*TSVs with top and bottom neighbors*" structure, while TSV-last is a "*TSVs with top, bottom and side neighbors*" structure, both obtained from [4]. We assume an equivalent single-dielectric environment in this experiment, as in [4]. And, the dielectric permittivity is set to 1. The side view and top view of the TSV-last structure are shown in Fig. 2, with detailed parameters in Table I. The keep-out-zone distance of TSV is set to 0.5 μm. In the MIV structure, a MIV is surrounded by a compact hexagon array of MIVs. The wire width equals to MIV diameter, and only three parallel wires are above or below the MIV array. The simulation has been performed with Synopsys Raphael [11]. Square approximation of an ITV is obtained by changing its circular cross section to a square with same area (i.e., square size $a = \sqrt{\pi} D/2$)[1]. The capacitances related to the center ITV are extracted.

From Table I, we can see that the square approximation overestimates the total capacitance by more than 5%. The error of coupling capacitances is much larger, often more than 20%. This verifies the necessity of modeling the ITV cylinders.

[1] We have done more experiments with the ITV cylinder replaced by its bounding box or its inscribed square prism. These two square-shape approximations both cause larger error than that using the same-area squares.

TABLE I. CAPACITANCE RESULTS FROM THE REAL CYLINDER MODEL AND AN APPROXIMATE SQUARE-SHAPE MODEL FOR THREE ITV STRUCTURES.

Structure	Dimensions(μm)					C_{total} (aF)		Err. C_{total} (%)	Error of C_{couple} (%)		
	TSV/MIV			Wire							
	D	h	s	w	t	Cylinder	Square		min	max	avg*
TSV-first	5	50	5	0.2	0.36	3740	3962	**5.9**	**-20**	**21**	**6.3**
TSV-last	5	50	5	0.2	0.36	3866	4065	**5.2**	**-38**	**71**	**13**
MIV	0.07	0.25	0.07	0.07	0.14	14.7	15.8	**7.5**	**-1.6**	**9.1**	**4.8**

* The average of the absolute values.

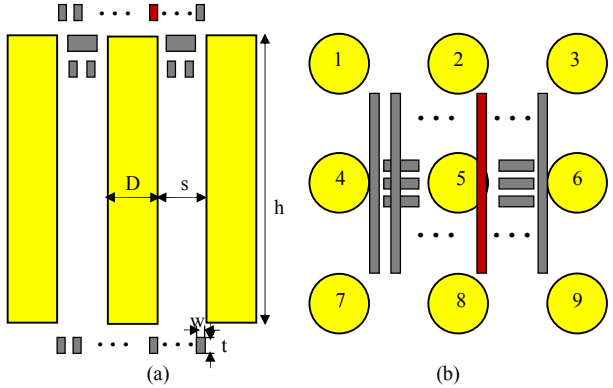

Fig. 2. The simulated TSV-last structure: (a) side view, (b) top view.

B. The Floating Random Walk Method

The FRW method for calculating electrostatic capacitance is originated from expressing the electric potential of a point $\boldsymbol{r}$ as an integral of the potential on surface S enclosing $\boldsymbol{r}$ [9, 12]:

$$\phi(\boldsymbol{r}) = \oint_S P(\boldsymbol{r}, \boldsymbol{r}^{(1)})\phi(\boldsymbol{r}^{(1)})\mathrm{d}\boldsymbol{r}^{(1)}, \quad (1)$$

where $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is called surface Green's function. The domain enclosed by S is often called the transition domain. $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is non-negative for any point $\boldsymbol{r}^{(1)}$ on S, and can be regarded as the probability density function (PDF) for selecting a random point on S. Therefore, $\phi(\boldsymbol{r})$ is the statistical mean of $\phi(\boldsymbol{r}^{(1)})$, and can be calculated with a Monte Carlo (MC) procedure.

To calculate the capacitances related to master conductor i, a Gaussian surface G_i is constructed to enclose it (see Fig. 3). According to the Gauss theorem, the charge of conductor i

$$Q_i = \oint_{G_i} F(\boldsymbol{r}) \int_{S^{(1)}} \omega(\boldsymbol{r}, \boldsymbol{r}^{(1)}) q(\boldsymbol{r}, \boldsymbol{r}^{(1)}) \phi(\boldsymbol{r}^{(1)}) \mathrm{d}\boldsymbol{r}^{(1)} \mathrm{d}\boldsymbol{r}, \quad (2)$$

where $F(\boldsymbol{r})$ is the dielectric permittivity at point $\boldsymbol{r}$, $q(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is the PDF for sampling on $S^{(1)}$ which may be different from $P(\boldsymbol{r}, \boldsymbol{r}^{(1)})$, and $\omega(\boldsymbol{r}, \boldsymbol{r}^{(1)})$ is the weight value [9]. Thus, Q_i can be estimated as the statistical mean of sampled values on G_i, which is further the mean of sampled potentials on $S^{(1)}$ multiplying the weight value. If the sampled potential is unknown, the construction of transition domain and the spatial sampling procedure will repeat until a point with known potential is obtained (e.g. on conductor surface). This forms a floating random walk (FRW) including a sequence of hops (see Fig. 3). Each hop is from the center of a transition domain to its boundary. With a number of such walks, the statistical mean of the weight values for the walks terminating at conductor j approximates the capacitance C_{ij} between conductors i and j (if $j \neq i$), or the total capacitance C_{ii} of master conductor i.

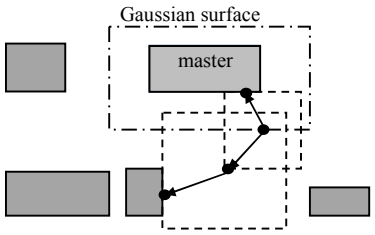

Fig. 3. Two examples of random walk in the FRW method for capacitance extraction (a 2-D top view).

Although the surface Green's function for a spherical transition domain has simple analytical expression, the cubic transition domain is widely adopted because it well fits the Manhattan-shaped interconnects in VLSI circuit [9]. This means larger probability for terminating a walk earlier. The sampling probability and weigh value for a cube domain can be pre-calculated and tabulated, so as to accelerate the sampling operation. Another technique is the space management [9, 10], which largely facilitates finding the nearest conductor for constructing the transition cube, especially for large structure.

The total runtime of the FRW method is roughly:

$$T_{total} = N_{walk} \cdot N_{hop} \cdot T_{hop}, \quad (3)$$

where N_{walk} is the number of random walks/paths, N_{hop} is the average number of hops per walk, and T_{hop} is the average computing time for a hop. The variance reduction techniques in [9] contributes to the reduction of N_{walk}, while suitable transition domains and efficient space management approach are crucial to the reduction of N_{hop} and T_{hop}, respectively.

III. FRW BASED TECHNIQUES FOR EXTRACTING THE CAPACITANCES OF STRUCTURE WITH CYLINDRICAL ITVS

In this section, we first present an extension of the FRW method to handle the cylindrical ITVs. Then, the technique which rotates the Manhattan transition cubes to reduce the number of hops is proposed. Finally, the problem of accelerating each hop for structures with a large number of ITVs is considered, followed by algorithm description and more discussions.

A. Walk with Manhattan Transition Cubes

Since the FRW method has very high efficiency to handle Manhattan geometries, a straightforward idea is still using "Manhattan" transition cubes but treating the ITV cylinder exactly. Here, "Manhattan" refers to a shape with each surface parallel to one of the *xoy*, *yoz*, and *zox* axis planes. We call this **FRW-1** method, which is a simple extension of the original FRW method.

For each hop of random walk, a maximum transition cube which does not intersect any conductor is needed. As in existing works, with the space management technique it is easy to find the nearest Manhattan conductor block. The ∞-norm distance between the current point of walk and the nearest block is the half edge size (HES) of a transition cube. However, this cube may intersect the cylinders and becomes invalid. To avoid this, we can further check all cylinders one by one, and shrink the cube once it crosses a cylinder. After that, we obtain the transition cube for performing a FRW hop.

Below, we show how to calculate the size of the valid transition cube while taking an ITV cylinder as the obstacle. Without loss of generality, we assume the cylinder's center is at (0, 0, 0), its diameter and height are D and h respectively. The current position if walk is (x, y, z). A vertical distance and a horizontal distance are calculated separately. And, the larger one of them is the HES of the Manhattan transition cube.

Firstly, it is easy to see that the vertical distance is

$$d_v = |z| - h/2 . \quad (4)$$

To calculate the horizontal distance we look at the 2D top view of a cylinder and a cube (i.e. a circle and a square). Two situations are shown in Fig. 4(a)~(b). If $-D/2 \le |x|-|y| \le D/2$, as in Fig. 4 (a), only a corner of the square touches the circle. The HES of the square, the horizontal distance d fulfills:

$$(|x|-d)^2 + (|y|-d)^2 = D^2/4 , \quad (5)$$

whose meaningful solution is:

$$d = (|x|+|y| - \sqrt{D^2/2 - (|x|-|y|)^2})/2 . \quad (6)$$

Otherwise, i.e. the situation shown in Fig. 4(b), the square touches the circle at an inner point of edge. In this case,

$$d = \max(|x|,|y|) - D/2 . \quad (7)$$

Combining (6) and (7), we get the horizontal distance d_{h1}:

$$d_{h1} = \begin{cases} \max(|x|,|y|) - D/2 , & \big|\,|x|-|y|\,\big| > D/2 \\ (|x|+|y| - \sqrt{D^2/2 - (|x|-|y|)^2})/2 , & \big|\,|x|-|y|\,\big| \le D/2 \end{cases} , \quad (8)$$

and

$$d_1 = \max(d_v, d_{h1}) \quad (9)$$

is the HES of the transition cube considering a specific cylindrical ITV.

In Fig. 4(a)~(b), we use green shadow to indicate the contact between the cylinder and the Manhattan transition cube. Its size is so small, if comparing with that in Fig. 3. Therefore, the random walk using Manhattan transition cube has less probability to terminate quickly, and is thus inefficient.

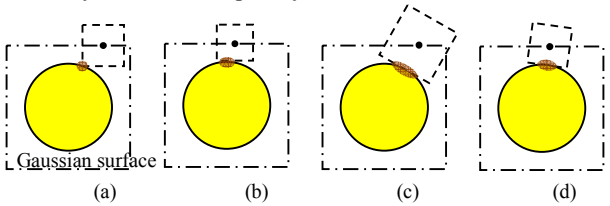

Fig. 4. 2D topologies of a cylindrical ITV and a Manhattan transition cube: (a), (b), or a rotated transition cube: (c), (d).

B. Walk with Rotated Transition Cubes

The FRW-1 method can be improved by allowing the transition cube to rotate in the *xoy* plane. This brings better touch to the cylinder [see Fig. 4(c)~(d)]. It increases the probability of terminating a walk, and reduces the number of hops. With this strategy, the horizontal distance or the HES of the transition cube can be:

$$d_{h2} = \sqrt{x^2 + y^2} - D/2 , \quad (10)$$

which is not less than d_{h1} in (8). However, the rotated transition cube may intersect other conductor, which should be avoided.

By traversing all the cylinders one by one and repeatedly calculating with (9), we get the final (also the smallest) Manhattan transition cube for performing a FRW hop. Suppose the final cube's size is limited by cylinder *A*. During this course, we can also get the second smallest transition cube which only intersects *A*. If the rotated transition cube with HES calculated with (10) is inside the second smallest cube, it should be accepted as a better transition domain (see Fig. 5). Otherwise, we still use the Manhattan transition cube.

A δ-touching criterion can be used to terminate a walk close to an ITV cylinder. That is, if the distance of the walking point is no more than $\delta \cdot D/2$ (δ is a small quantity), we regard that the walk has reached the cylinder (see Fig. 5). If the rotated transition cube is used, this can be applied more efficiently. We can calculate the largest distance from the cube's touching face to the cylinder. If it is no more than $\delta \cdot D/2$ (equivalently $d_{h2} \le D/2 \cdot \sqrt{\delta(2+\delta)}$), any hop to that face makes the walk terminated, which has a fixed 1/6 probability. Now, we get a method with rotated transition cubes (called **FRW-2**).

In the above discussion, we traverse all cylindrical ITVs in each hop. If there are many ITVs in the extracted structure, T_{hop} will be very large, which greatly harms the algorithm's runtime.

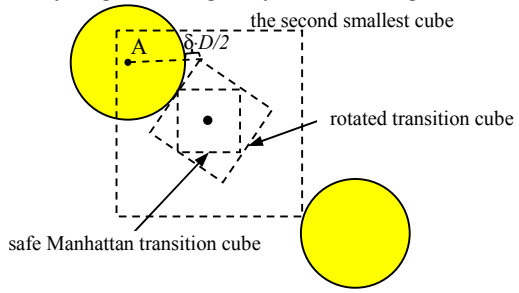

Fig. 5. The rotated transition cube is a better choice.

C. Reduce the Time for Each Hop

To reduce T_{hop} for the situation where a large number of cylindrical ITVs are involved, we consider the space management technique. Firstly, we can insert each ITV's Manhattan bounding box into the space management structure [9]. This does not induce any modification of the existing approach. Therefore, we can easily find the nearest block from current walking point. This block is either a regular conductor or an ITV's bounding box. If it's the former, the transition cube is constructed normally. For the latter case, we have to consider the ITV cylinder and perform further computation.

When the nearest block is an ITV's bounding box, we may be able to find a larger transition domain touching the ITV's cylinder. According to (9) and (10), we can construct two transition cubes touching the ITV with edge sizes L_1 and L_2 respectively. Obviously, $L_2 \ge L_1$. However, the both may not be safe (may intersect other conductor). To ensure the safety, we can find the second nearest conductor block and construct a Manhattan transition cube (with size L_3) touching it. It does not matter if the block is an ITV's bounding box. We now choose one from the three transition cubes. If $L_3 < L_1$, we have to choose the third transition cube to avoid crossing any conductor [see Fig. 6(a)]. Otherwise, we judge the condition $(|\cos(\theta)| + |\sin(\theta)|)L_2 \le L_3$, where θ is the rotation angle of the rotated transition cube. If it's true, we can choose the second transition cube which is inside the third one and is safe [see Fig. 6(b)]. If the condition does not stand, the rotated transition

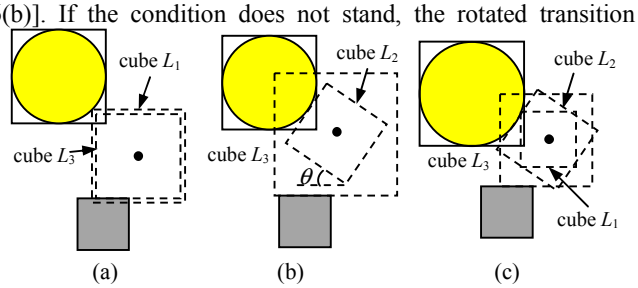

Fig. 6. Construct transition domain according to the nearest cylinder and the second nearest block.

cube cannot be accepted. We have to choose the safe first transition cube with size L_1. This situation is shown in Fig. 6(c). Note that, if the chosen cube's size is zero, the current point must be on the cylindrical surface and we terminate the walk.

The left problem is how to find the second nearest block without traversing the cylindrical ITVs one by one. We can define each ITV's neighbor region by expanding distance d_{nb} based on its bounding box (see Fig. 7). In the initialization of space management [10], we treat ITV's neighbor region as a special spatial cell and generate a candidate list containing the possible nearest blocks from any points in it. The only difference is that the ITV itself is not inserted into the candidate list. During the hop, when current point's nearest block is an ITV's bounding box, we first check if it is in the ITV's neighbor region. If it is (see point P_1 in Fig. 7), we can easily get the second nearest block with a pre-calculated candidate list. However, if the point is out of the neighbor region (see P_2 in Fig. 7) the second nearest block cannot be found. In this situation, we just use the Manhattan transition cube restricted by the ITV's bounding box, whose HES is larger than d_{nb}. By setting a suitably large d_{nb}, it is guaranteed that we either get the second nearest block efficiently or use a large enough transition cube. This largely reduces the time of performing a hop while handling the structure with a large number of cylindrical ITVs.

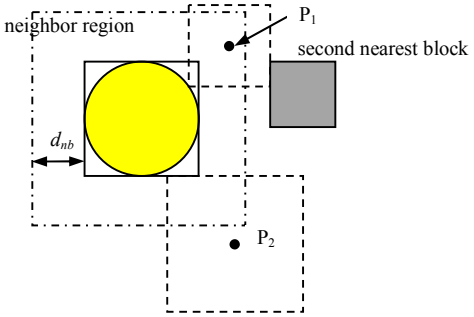

Fig. 7. A cylindrical ITV's neighbor region.

D. Algorithm Flow and Discussions

With the technique in last subsection, we obtain method **FRW-3** for extracting the capacitances for a structure with cylindrical ITVs. With this method, the flow of performing a FRW walk can be described as the following Algorithm 1.

Algorithm 1: A FRW walk in the FRW-3 method (startPoint P)

1. B := the nearest conductor block (or ITV bounding box) from *P*;
2. d := *d*(P, B); *IsRotated* := false;
3. **If** B isn't an ITV's bounding box **then goto** Step 16; **Endif**
4. Use V to denote the cylindrical ITV inside B;
5. **If** d > ITV's d_{nb} **then goto** Step 16; **Endif**
6. d := d_1(P, V); // calculate with (9) in **FRW-1**.
7. S := *d*(P, the nearest block found from V's candidate list);
8. **If** S < d **then**
9. d := S; **goto** Step 16;
10. **Endif**
11. L := $d_{h2}(P, V)$; // calculate with (10).
12. Get θ, which is the rotation angle of the transition cube;
13. **If** d < L and (|cos(θ)|+|sin(θ)|)L < S **then**
14. d := L; *IsRotated* := true;
15. **Endif**
16. **If** d < a small tolerance **then**
17. This walk terminates at conductor B or V; **return.**
18. **Endif**
19. Use *d* as the HES to construct a Manhattan transition cube;
20. **If** *IsRotated*, **then** rotate the transition cube by θ; **Endif**
21. *P* := a randomly selected point on the transition cube;
22. **goto** Step 1;

The function *d*(,) in Steps 2 and 7 calculates the ∞-norm distance between a point and a 3D Manhattan block. Steps 11 and 12 determine a rotated transition cube.

A whole description of FRW-3 is given as Algorithm 2.

Algorithm 2: The FRW-3 algorithm for structure with cylindrical ITVs

1. Load pre-computed transition probabilities and weight values;
2. Construct the Gaussian surface enclosing master conductor *i*;
3. C_{ij} :=0, ∀*j*; *npath* := 0;
4. **Repeat**
5. *npath*: = *npath*+1;
6. Pick a point $\boldsymbol{r}$ on the Gaussian surface, and generate a cubic transition domain S centered at $\boldsymbol{r}$; pick a point $\boldsymbol{r}^{(1)}$ on the surface of S with the transition probabilities and then calculate the weight value ω with the pre-computed data;
7. Perform a walk starting from $\boldsymbol{r}^{(1)}$; //Algorithm 1
8. C_{ij} := C_{ij} +ω ; //the walk terminates at conductor *j*
9. **Until** the convergence criterion is met
10. C_{ij} := C_{ij} /*npath*, ∀*j*.

In the FRW-3 algorithm, no assumption of the number, size, and positions of ITVs is made. We only assume that the Manhattan bounding box of an ITV does not intersect other conductor block or ITV's bounding box. In realistic layouts, this is obviously satisfied.

The proposed techniques hardly degrade the accuracy of the original FRW algorithm. Only the δ-touching criterion in Section III.B introduces some error. In practice, we set δ to 5×10^{-4}, which keeps the induced error in the order of 0.1% [16].

As described in Section III.C and Algorithm 1, the FRW-3 method performs extra computation for generating rotated transition cube only when the current point is close to an ITV. The space management is also a small modification of the existing techniques [9, 10]. Therefore, the increase of computational cost should be limited as compared with the original FRW algorithm which only handles Manhattan objects.

Because the cubic transition domains are still used, the proposed method can be easily extended to the problem with multi-layered dielectrics. It can be accomplished by plugging in the pre-characterized multi-dielectric GFTs and WVTs as [9].

IV. Numerical Results

We have implemented the FRW method and the proposed techniques in C++. The space management technique in Section III.C is implemented based on an Octree structure and the pruning skills in [10], and d_{nb} for the ITV's neighbor region is set to the radius of ITV. Several 3D-IC structures with TSVs or MIVs are tested. We first use several small and medium test cases to validate the accuracy and efficiency of the proposed method. Raphael [11] which employs FDM with dense discretization is used to validate the accuracy, while RWCap [9, 10] which only handles Manhattan geometries is used for efficiency comparison. Then, large cases and multi-dielectric

cases are used to validate the scalability and versatility of the proposed techniques, respectively. The results of two fast BEM solvers, i.e. FastCap [13] and QBEM [14], are also presented for comparison.

Experiments are carried out on a Linux server with Intel Xeon E5-2650 2.0 GHz CPU. All results are obtained from the execution of serial computing.

A. Results for Small and Medium Cases

Four structures are tested, and three of them are those described in Table I. The last one "TSV-first2" is the same as "TSV-first", except that TSVs No. 1, 3, 7, 9 and several horizontal wires are removed (see Fig. 2). For each case, the total capacitance of the center ITV is first extracted. The results obtained with Raphael, RWCap and our FRW method (setting 1-σ error to be 0.5% of the mean value) are listed in Table II. From it we see that the discrepancy between the result of our method and the Raphael's result got from accurately modeling cylinder shape is **within 1.5%**. The result of RWCap is close to the Raphael's result based on the square approximation, which causes **from 5.1% to 7.5% error** on the total capacitance of ITV. While comparing the runtime of RWCap and our method, we see that the latter is 3X~6X slower.

To evaluate the accuracy of the proposed method for extracting coupling capacitance, we present a result in Table III. For the TSV structures, it is the coupling capacitance between the center TSV and a horizontal wire (the red one in Fig. 2), while for the MIV structure it is the coupling between the center MIV and a neighbor MIV. When running the FRW algorithms, we set the horizontal wire as the master conductor and the 1-σ error of the coupling capacitance to 1% of its mean value for termination. From Table III, we can see the large error brought by the square-shape approximation (**over 20% error** in the TSV cases, and **8.7% error** in the MIV case). And, the proposed method exhibits high accuracy as compared with Raphael's result with cylinder model. For the runtime, the proposed method only increases 30% computing time of that consumed by RWCap for the TSV structures. Because there are much fewer TSVs than the horizontal wires, the runtime overhead of the proposed method is moderate.

FastCap and QBEM are also run with the ITV and the horizontal wire set as the master conductor, respectively. Their computational results are listed in Table IV and Table V. To make the computation feasible, each cylinder is approximated by a regular 16-side prism and the cylindrical surface is replaced by 16 rectangles. The approximation with regular 32-side prisms has also been tried, which produces similar results. In the tables, "Err" denotes the error measured based on Raphael's result. We can see that FastCap has good accuracy on the total capacitance, but is quite inaccurate on the TSV related coupling capacitance (see Table V). Note in these cases, there are TSVs with large dimensions and a number of horizontal wires. So, the panel discretization employed in FastCap may not dense enough for producing accurate coupling capacitance. We have tried denser discretization, but FastCap broke down due to its limitation of 2GB memory usage. On the other hand, QBEM employs an automatic boundary discretization and is able to extract the total and coupling capacitances to certain accuracy. The error of QBEM's result may be due to the 16-side prism approximation and the imperfect quality of boundary discretization mesh.

From Table IV and Table V, we can see that the proposed FRW algorithm consumes comparable or even more time than the fast BEM solvers while extracting the capacitance of the small MIV case (including only 13 conductors). However, for the TSV cases, our algorithm is **more than 10X faster** than the latter while extracting the coupling capacitance accurately. The speedup ratio in the total-capacitance extraction is less, but is still about 6X and 30X compared to FastCap and QBEM respectively. Generally, the runtime speedup of our method increases with increasing size of test case.

For the test cases with the single dielectric assumption, the memory cost of our FRW algorithm is no more than 1MB. It is negligible if compared with the memory needed by the BEM solvers (see Tables IV and V).

TABLE II. THE RESULTS OBTAINED FROM EXTRACTING AN ITV'S TOTAL CAPACITANCE (IN UNIT OF AF).

Case	Raphael			RWCap		Proposed FRW Alg.		
	cylinder	square	Err(%)	C_{tot}	Time(s)	C_{tot}	Err(%)	Time(s)
TSV-first	3740	3962	**5.9**	3930	2.06	3778	**1.0**	13.4
TSV-last	3866	4065	**5.1**	4056	2.01	3908	**1.1**	12.7
MIV	14.7	15.8	**7.5**	15.6	0.61	14.9	**1.4**	1.88
TSV-first2	3718	3939	**5.9**	3916	2.58	3776	**1.5**	15.5

TABLE III. THE RESULTS OBTAINED FROM EXTRACTING AN ITV RELATED COUPLING CAPACITANCE (IN UNIT OF AF).

Case	Raphael			RWCap		Proposed FRW Alg.		
	cylinder	square	Err(%)	C_c	Time(s)	C_c	Err(%)	Time(s)
TSV-first	49.9	60.2	**20.6**	59.6	3.5	50.3	**0.8**	4.51
TSV-last	48.2	58.6	**21.6**	58.2	4.2	48.1	**-0.2**	5.43
MIV	2.06	2.24	**8.7**	2.26	2.6	2.1	**1.9**	8.01
TSV-first2	50	60.4	**20.8**	60.0	3.9	49.6	**-0.8**	5.14

TABLE IV. THE COMPARISION OF THE FAST BEM SOLVERS AND OUR METHOD FOR THE TOTAL-CAPACITANCE EXTRACTION.

Case	FastCap					QBEM					Proposed FRW Alg.					
	C_{tot}(aF)	Err(%)	#panel	Time(s)	Mem.	C_{tot}(aF)	Err(%)	#panel	Time(s)	Mem.	C_{tot}(aF)	Err(%)	Time(s)	Sp1*	Sp2*	Mem.
TSV-first	3710	-0.8	190K	67.3	1.8GB	3603	-3.7	118K	402	7.6GB	3778	1.0	13.4	**5.0**	**30**	~1MB
TSV-last	3736	-3.4	197K	79.0	1.9GB	3708	-4.1	118K	404	7.7GB	3908	1.1	12.7	**6.2**	**32**	~1MB
MIV	14.7	0.0	40K	8.43	407MB	14.33	-2.5	6.5K	1.58	48MB	14.9	1.4	1.88	**4.5**	**<1**	<1MB
TSV-first2	3691	-0.7	117K	50.1	1.1GB	3547	-4.6	82K	271	5.3GB	3776	1.5	15.5	**3.2**	**17**	~1MB

*Sp1 and Sp2 are the speedup ratios to FastCap and QBEM, respectively.

TABLE V. THE COMPARISION OF THE FAST BEM SOLVERS AND OUR METHOD FOR THE COUPLING-CAPACITANCE EXTRACTION.

Case	FastCap					QBEM					Proposed FRW Alg.					
	C_c(aF)	Err(%)	#panel	Time(s)	Mem.	C_c(aF)	Err(%)	#panel	Time(s)	Mem.	C_c(aF)	Err(%)	Time(s)	Sp1*	Sp2*	Mem.
TSV-first	64.9	**30.1**	190K	66.8	1.8GB	48.0	-3.8	109K	298	5.9GB	50.3	0.8	4.51	**15**	**66**	~1MB
TSV-last	64.5	**33.8**	197K	79.1	1.9GB	46.1	-4.4	110K	299	6.0GB	48.1	-0.2	5.43	**15**	**55**	~1MB
MIV	2.11	2.4	40K	8.23	407MB	2.06	0.0	6.5K	1.58	48MB	2.1	1.9	8.01	**1.0**	**<1**	<1MB
TSV-first2	65.1	**30.3**	117K	51.2	1.1GB	47.9	-4.2	85K	192	4.2GB	49.6	-0.8	5.14	**10**	**37**	~1MB

*Sp1 and Sp2 are the speedup ratios to FastCap and QBEM, respectively.

B. Results for Large Cases

To test the proposed FRW based techniques for large-scale structures, four large cases with more ITVs are constructed:

- **viafirst100**: a random placement of 100 TSVs of diameter 4μm and height 40μm, plus a top and bottom layers of parallel wires. The wire dimensions follow those in Case TSV-first; the spacing between any two TSVs is kept to be larger than 4μm.
- **viafirst400**: the structure is similar to that of viafirst100, except that the random TSV placement includes 400 TSVs.
- **MIV144**: a regular layout of transistor-level monolithic 3D IC, with 144 MIVs (see Fig. 8). The dimensions of MIV and wires are the same as those in Case MIV. There are parallel wires in the very top and bottom metal layers.
- **MIV576**: formed by duplicating case MIV144 for four times.

For these large cases with at least 100 cylindrical ITVs and 350 wires, it becomes infeasible to simulate them with Raphael. The FastCap program [13] has a limitation of 2GB memory usage, and is not able to simulate them either.

For each case, we set a net of ITV as the master conductor and extract the capacitances (a MIV net is outlined in Fig. 8). The results of QBEM and our FRW method are given in Table VI, where QBEM's results for the two largest cases are not available due to the issue of memory overflow. From Table VI we can see that the proposed method can be up to **180X faster** than QBEM, while the capacitance results of both methods are comparable.

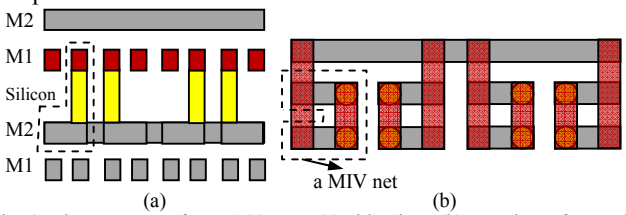

Fig. 8. The structure of MIV144 case: (a) side view, (b) top view of a small part of layout with 8 MIVs (the parallel wires in the very top and bottom layers are not drawn).

The proposed method (FRW-3) is also compared with the simple extension of the original FRW using Manhattan transition cube (FRW-1) and the algorithm without the proposed space management technique (FRW-2). Their results are listed in Table VII. Comparing the average numbers of hops per walk (N_{hop}) in FRW-1 and FRW-2, we see that the rotated transition cube can reduce the hop number by more than 2X. And, FRW-3 is much faster than FRW-2, because with the space management T_{hop} can be largely reduced. The speedup ratio of FRW-3 over the simple extension of the original FRW reaches **20X** for the largest structure.

We have also extracted the capacitances of a wire net. The results reveal the similar speedup of FRW-3 over FRW-1. It should be pointed out that the runtime for extracting a wire's capacitances can be much less than that for extracting the TSV's capacitances. It is due to two reasons: 1) the electric field is much uniform around a wire than that around a big TSV, and thus N_{walk} in FRW is much fewer in the former situation; 2) the FRW walk in the former situation seldom encounters the cylinder TSV, and thus can be performed faster.

TABLE VI. THE RESULTS OF QBEM AND THE PROPOSED FRW METHOD FOR EXTRACTING LARGE CASES.

Case	QBEM					Proposed FRW Alg.			
	C_{tot}(fF)	Dis.(%)	#panel	Mem.	Time(s)	C_{tot}(fF)	Mem.	Time(s)	Sp.
MIV144	0.509	-5.9	27K	549MB	25	0.541	1MB	1.4	**18**
MIV576	0.515	-5.0	78K	5.2GB	270	0.542	3MB	1.5	**180**
Viafirst100	--	--	--	--	--	3.03	7MB	35.3	--
Viafirst400	--	--	--	--	--	3.04	29MB	35.0	--

TABLE VII. THE RESULTS OF FRW ALGORITHMS FOR FOUR ITV STRUCTURES (TIME IN UNIT OF SECOND).

Case	FRW-1			FRW-2			FRW-3				
	N_{walk}	N_{hop}	Time	N_{walk}	N_{hop}	Time	N_{walk}	N_{hop}	Time	Sp1*	Sp2*
MIV144	148K	13.0	3.2	149K	10.8	2.7	152K	11.2	1.4	**2.3**	1.9
MIV576	149K	13.0	11.4	147K	10.8	9.4	152K	11.2	1.5	**7.7**	6.4
Viafirst100	6.3M	36.0	231	6.2M	13.3	96.0	6.2M	11.5	35.3	**6.5**	2.7
Viafirst400	6.1M	36.0	710	6.1M	13.2	279	6.2M	11.5	35.0	**20**	8.0

*Sp1 and Sp2 are the speedup ratios to FRW-1 and FRW-2, respectively.

C. Results for Multi-Dielectric Cases

For the test cases with TSVs, we assume there are ILDs with relative permittivities of 3.7 and 4.2. For the cases with MIVs, the ILD permittivities are set to 2.6 and 5.0. With the permittivity of silicon set to 11.9, we get the multi-dielectric counterparts for the test cases. Here, TSV's liner is ignored, because it is very thin and can be well modeled with the equivalent dielectric formula in [4]. With the TechGFT program [9], we have built the GFTs and WVTs for the multi-dielectric structures, which are needed by the FRW algorithms. The results of Raphael, QBEM and our method are listed in Table VIII. Due to the memory issue, FastCap breaks down for these multi-dielectric cases. Similarly, the results of Raphael and QBEM are also not available for some larger cases. Due to the quasi-multiple medium approach, we notice that QBEM is more suitable for multi-dielectric structures than FastCap [14].

The results in Table VIII verify the accuracy of our method again. The increase of memory used by the FRW method is due to the multi-dielectric GFTs and WVTs. The speedup ratio of proposed method to QBEM **is up to 61X**. Different versions of the FRW algorithms for cylindrical ITVs have also been compared. As the results in Table VII for single-dielectric cases, we see similar acceleration of the proposed techniques for the multi-dielectric cases (e.g. the largest speedup of 19.3X for the largest case).

TABLE VIII. THE RESULTS OF RAPHAEL, QBEM AND OUR FRW METHOD FOR THE MULTI-DIELECTRIC STRUCTURES (CAPACITANCE IN UNIT OF FF).

Case	Raphael	QBEM			Proposed FRW Alg.				
	Cap.	Cap.	Mem.	Time(s)	Cap.	Err(%)	Mem.	Time(s)	Sp.
TSV-first	33.4	32.56	11GB	534	33.9	1.5	22MB	28.5	**19**
TSV-last	32.9	30.96	5.2GB	188	33.2	0.9	22MB	32.7	**5.9**
MIV	0.146	0.146	581MB	18.4	0.148	1.4	22MB	2.53	**7.3**
TSV-first2	32.9	31.88	8.8GB	400	33.5	1.9	22MB	48.0	**8.3**
MIV144	--	0.276	856MB	35.9	0.292	--	23MB	6.31	**5.7**
MIV576	--	0.29	6.7GB	344	0.291	--	25MB	5.67	**61**
Viafirst100	--	--	--	--	24.7	--	28MB	112	**--**
Viafirst400	--	--	--	--	25.2	--	51MB	71.9	**--**

V. CONCLUSIONS

To tackle the challenge of accurate parasitic extraction brought by high-density ITVs (TSVs and MIVs) in 3D ICs, efficient techniques based on the floating random walk method are proposed to calculate the electrostatic capacitances among cylindrical ITVs and wires. The proposed method is accurate and versatile, and shows advantages over the fast capacitance solvers based on boundary element method. The collaboration of this work and the ITV model considering semiconductor effect could be explored in the future.

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