

Utilizing Macromodels in Floating Random Walk Based Capacitance Extraction

Wenjian Yu[†], Bolong Zhang[†], Chao Zhang[†], Haiquan Wang[†], Luca Daniel[‡]

[†]Dept. Computer Science & Technology, Tsinghua University, Beijing 100084, China. [‡]Dept. of EECS, MIT, Cambridge, MA 02139, USA. Email: yu-wj@tsinghua.edu.cn, {blzhang.m, eric.3zc}@gmail.com, w2009fxtx@163.com, dluca@mit.edu

Abstract—This paper presents techniques that use macromodels in order to extend and improve the floating random walk (FRW) method for capacitance extraction. A macromodel is built for each sub-structure for which it is necessary or convenient to hide its geometry details during capacitance extraction. Then, a macromodel-aware random walk scheme connects the Markov-chain random walk inside the macromodels and the FRW outside through scalable blank patch regions. This method can be used for instance to extract capacitances for structure with encrypted sub-structures, and extend the FRW method’s capability for structure with complex geometry or repeated layout patterns. Numerical results validate the merits of the proposed method with structures including encrypted FinFET layout, complex geometry features, and cyclic layout patterns.

I. INTRODUCTION

The microfabrication process technology of integrated circuits (ICs) has recently evolved into the era of nanometer scale. To continue Moore’s law, novel device structures have been invented [1], generating complex interconnect/device geometries and dielectric profiles. This structure complexity includes conformal dielectrics and non-Manhattan metal/dielectric shapes caused by side-tangent effect, end-rounding effect, etc. and it causes difficulty to existing methods for capacitance extraction. On the other hand, with decreased performance margin, more accuracy on capacitance extraction is required to keep reasonable time-to-market and production yield of ICs. Accurate capacitance extraction for the nanometer IC structures has become a key challenge in the validation of process technologies and in the verification of IC designs.

A lot of field-solver techniques have been proposed for accurate capacitance extraction [2]. They can be classified into three categories: 1) domain discretization method, including finite difference method (FDM) and finite element method (FEM) [3, 4], 2) boundary element method (BEM) [5–8], and 3) the floating random walk (FRW) method [9–14]. The first two classes of methods involve volume or surface discretization and result in a system of linear equations. On the contrary, the FRW method is based on the Monte Carlo method, and has the advantages of more scalability for very large structures, reliable and tunable accuracy, better parallelism, and much smaller memory usage [12, 13].

With the advent of parallel computing techniques, the FRW method has become popular and widely used in various capacitance extraction tasks. However, the FRW method’s efficiency mainly depends on the assumption that the handled geometries are all rectilinear-shaped. To handle the emerging non-Manhattan geometries, Manhattan geometry approximation is typically applied which often results in loss of accuracy.

Complicated dielectric profile also brings difficulties. Approaches such as those in [12, 14] have been proposed, but they become inefficient or inaccurate when the structure includes many dielectrics or non-planar conformal dielectrics. On the other hand, fast BEM or FEM capacitance solvers are more naturally capable of handling the complexity of geometries or dielectric profiles. Existing work has revealed that such techniques do not present specific issue when extracting complex non-Manhattan and multi-dielectric structures [5, 6].

Another challenge in capacitance extraction is the need of encrypting the structure information from foundry or IP vendor. In order to perform accurate extraction at the advanced technology nodes, the foundry must provide complete information of devices (geometry and dielectric parameters). Similarly, the layout details of an IP block is needed for accurately extracting the capacitances around it. However, the foundry and IP vendor need to protect their trade secrets by hiding the sensitive structure information. This causes a contradiction. An intuitive idea for solving this problem is to build a macromodel for certain regions chosen by the foundry or IP vendor. A FDM based macromodeling technique was recently proposed for encrypting structure information for capacitance extraction [15]. However, it cannot be utilized by the state-of-the-art capacitance solvers based on FRW method or BEM. Actually, the macromodeling technique has been there for a long time [7], but it was previously created for extending the capacity or reducing the runtime of capacitance field solvers [8].

The aim of this work is to combine the macromodeling technique and the state-of-the-art FRW method for capacitance extraction. By proposing a macromodel-aware random walk algorithm, we extend and improve the usage of FRW method in different scenarios. Our contributions are as follows.

1) A new random walk algorithm, which utilizes the macromodels and is able to handle general three-dimensional (3-D) layout structures, is proposed. Its main idea is to connect the Markov-chain random walk (MCRW) inside the macromodel and the FRW outside through a pre-characterized patch region. The algorithm can be used for the capacitance extraction with encrypted structures, while inheriting the advantages of the FRW based capacitance solver.

2) Besides the problem of sensitive structure encryption, we propose to apply the macromodel-aware random walk algorithm also to problems including complex geometry (such as conformal dielectric, non-Manhattan metal shape, etc.) and repeated layout patterns. Numerical results demonstrate the feasibility and efficiency of our method. Particularly, it can bring over **10X** speedup for the extraction of structures with repeated layout patterns.

It should be pointed out that a similar work exists, where

the macromodels built by BEM and a random walk process is combined [11]. However, that work was targeted to the topological-variation aware capacitance extraction where the layout is made of a combination of predefined motifs (sub-structures). For a general 3-D problem, it is infeasible to decompose the layout into pieces and build a macromodel for each piece, due to huge time and memory cost. And if only a portion of simulated structure has corresponding macromodels, as considered in this work, the method in [11] becomes invalid.

II. BACKGROUND

A. The Floating Random Walk Method

The FRW method for calculating capacitances is originated from expressing the electric potential of a point \mathbf{r} as an integral on surface S surrounding it [9, 12]:

$$\phi(\mathbf{r}) = \oint_S P(\mathbf{r}, \mathbf{r}^{(1)})\phi(\mathbf{r}^{(1)})d\mathbf{r}^{(1)}, \quad (1)$$

where $\phi(\mathbf{r})$ is the potential of point \mathbf{r} and $P(\mathbf{r}, \mathbf{r}^{(1)})$ is called surface Green's function. The domain enclosed by S is called transition domain. $P(\mathbf{r}, \mathbf{r}^{(1)})$ can be regarded as a probability density function (PDF). With the Monte Carlo method, $\phi(\mathbf{r})$ can be estimated as the statistical mean of $\phi(\mathbf{r}^{(1)})$.

When computing the capacitances related to a master conductor i , one should first construct a Gaussian surface G_i enclosing it (see Fig. 1). According to the Gauss theorem, the charge of conductor i is:

$$Q_i = \oint_{G_i} F(\mathbf{r})g \oint_{S^{(1)}} \omega(\mathbf{r}, \mathbf{r}^{(1)})\tilde{P}(\mathbf{r}, \mathbf{r}^{(1)})\phi(\mathbf{r}^{(1)})d\mathbf{r}^{(1)}d\mathbf{r}, \quad (2)$$

where $F(\mathbf{r})$ is the dielectric permittivity at point \mathbf{r} , $\tilde{P}(\mathbf{r}, \mathbf{r}^{(1)})$ is the PDF for sampling on $S^{(1)}$ which may be different from $P(\mathbf{r}, \mathbf{r}^{(1)})$, and $\omega(\mathbf{r}, \mathbf{r}^{(1)})$ is the weight value [9, 12]. Thus, Q_i can be estimated as the statistical mean of sampled values on G_i , which is further the mean of sampled potentials on $S^{(1)}$ multiplying the weight value. If the potential of a sample point $\mathbf{r}^{(1)}$ is unknown, Eq. (1) is substituted into (2) recursively. The computation can be described as a floating random walk (FRW) procedure. The walk starts from the Gaussian surface, and repeatedly jumps from a transition domain's center to its surface, until reaching conductor surface. After performing a number of walks, the statistical mean of the weight values for the walks terminating at conductor j approximates the capacitance C_{ij} between conductors i and j .

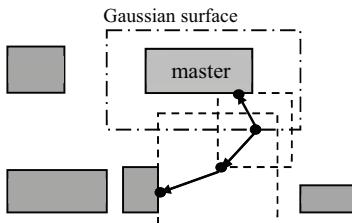


Fig. 1: Two examples of random walk in the FRW method for capacitance extraction (a 2-D top view).

The cubic transition domain is widely adopted because it fits well the Manhattan-shaped interconnects in VLSI circuit [12]. This means larger probability for terminating a walk earlier. The sampling probability and weight value for a cube domain can be pre-calculated and tabulated, so as to accelerate the sampling operation. Besides, space management techniques [13] are useful for quickly finding the nearest conductor for

constructing the transition cube, especially for simulating a large structure including thousands of conductor blocks.

The total runtime of the FRW method is roughly:

$$T_{total} = N_{walk} \times N_{hop} \times T_{hop}, \quad (3)$$

where N_{walk} is the number of random walks or paths, N_{hop} is the average number of hops per walk, and T_{hop} is the average computing time for a hop. The variance reduction techniques in [12] contributes to the reduction of N_{walk} , while the space management technique are crucial to the reduction of T_{hop} .

B. Building Macromodel for a Sub-Structure

The macromodel for capacitance extraction is essentially a matrix which reflects the electrostatic field couplings within a sub-structure produced by partitioning the problem domain. It can be built using FDM or BEM, and was invented for the global hierarchical capacitance extraction [7, 8]. Below, we briefly introduce the procedure of building macromodels using BEM.

For a homogeneous 3-D sub-domain (sub-structure) Ω , the direct boundary integral equation (BIE) holds [6]:

$$\frac{1}{2}u_s + \oint_{\partial\Omega} q_s^*(\mathbf{r})u(\mathbf{r})d\mathbf{r} = \oint_{\partial\Omega} u_s^*(\mathbf{r})q(\mathbf{r})d\mathbf{r}, \quad (4)$$

where $u(\mathbf{r})$ and $q(\mathbf{r})$ are the electric potential and normal electric field intensity at point \mathbf{r} on domain boundary $\partial\Omega$. u_s is the potential at a point s on the boundary $\partial\Omega$. $u_s^*(\mathbf{r}) = 1/4\pi |\mathbf{r} - \mathbf{s}|$ is the free-space Green's function associated with point s , and $q_s^*(\mathbf{r})$ is its derivative along the outward normal direction of boundary. Employing constant quadrilateral or triangular discretization elements and evaluating the direct BIE at N points, one for each element (collocation method), we obtain N discretized BIEs. After evaluating the integrals on each elements, one obtains the matrix equation:

$$\mathbf{H}\mathbf{u} = \mathbf{G}\tilde{\mathbf{q}}, \quad (5)$$

which leads to $\mathbf{G}^{-1}\mathbf{H}\mathbf{u} = \tilde{\mathbf{q}}$. Here \mathbf{u} and $\tilde{\mathbf{q}}$ are vectors of potential and normal electric field intensity on the elements, respectively. Thus, the BEM macromodel [7, 8] is obtained:

$$\mathbf{A} = \mathbf{G}^{-1}\mathbf{H}, \quad (6)$$

which we call boundary potential-flux matrix (BPFM).

The macromodels used in [11], where it was called Markov transition matrix (MTM), is slightly different. With a diagonal matrix \mathbf{D} including the products of boundary element area and dielectric permittivity, we get:

$$\mathbf{H}\mathbf{u} = \mathbf{G}\mathbf{D}^{-1}\mathbf{D}\tilde{\mathbf{q}} = \mathbf{G}\mathbf{D}^{-1}\mathbf{q}, \quad (7)$$

where \mathbf{q} stands for a vector of electric charge on boundary elements. So, the MTM is obtained as [11]:

$$\mathbf{C} = \mathbf{D}\mathbf{G}^{-1}\mathbf{H}, \text{ where } \mathbf{Cu} = \mathbf{q}. \quad (8)$$

It defines the relationship between electric potential and charge. Therefore, we call \mathbf{C} in (8) boundary potential-charge matrix (BPCM). It is equivalently the capacitance matrix in a closed domain, and is referred to macromodel thereafter.

Note that boundary $\partial\Omega$ includes conductor surface if there is conductor in domain Ω . So, the BPCM \mathbf{C} includes all capacitances among the elements on both conductor surface and domain outer boundary. Because the boundary elements on a same conductor have same potential, we just need one potential and one charge variable for a conductor. In [8], this idea was employed to condense the size of BPFM. In this work, we apply this condensing technique to BPCM, so that each conductor corresponds to one index in matrix \mathbf{C} .

C. Markov Chain Based Random Walk

A hierarchical random walk (HRW) method has been proposed for a fabric-aware extraction problem [11]. In that problem, each simulated structure is a composition of predefined motif structures. The BPCM is pre-calculated for each motif. Based on these BPCMs, a Markov-chain random walk (MCRW) scheme was then proposed. Suppose that one wants to calculate the coupling capacitances between conductor i in motif 1 and other conductors (see Fig. 2). Without loss of generality, one can assume that conductor i has index i in the BPCM for motif 1. Then, the charge of conductor i

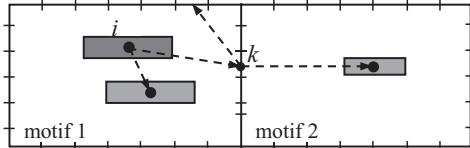


Fig. 2: The illustration of Markov-chain random walks in a motif and across motif interface.

$$Q_i = \sum_{j=1}^{N_1} C_{ij}^{(1)} U_j^{(1)}, \quad (9)$$

where $\mathcal{C}^{(1)}$ is motif 1's BPCM (an $N_1 \times N_1$ matrix), $U_j^{(1)}$ is the potential of motif 1's j -th element. From (9), we have

$$Q_i = \left(-C_{ii}^{(1)}\right) \frac{\sum_{j=1}^{N_1} -C_{ij}^{(1)} U_j^{(1)}}{C_{ii}^{(1)}} = \left(-C_{ii}^{(1)}\right) \sum_{j=1, j \neq i}^{N_1} -\frac{C_{ij}^{(1)}}{C_{ii}^{(1)}} U_j^{(1)}, \quad (10)$$

assuming the potential at conductor i is 0 ($U_i^{(1)} = 0$). Under this assumption, Q_i equals to the coupling capacitance between i and another unique conductor set 1 Volt potential. Note that item $-C_{ij}^{(1)}/C_{ii}^{(1)}$ in (10) represents the probability for random transition from conductor i to some other conductor or boundary element j of motif 1 [11]. Eq. (10) suggests a kind of Markov-chain random walk starting from conductor i , and $-C_{ii}^{(1)}$ is like the weight value in the FRW method. If the walk stops at a boundary element (with unknown potential), the following derivation will help to continue it until touching a conductor (with constant potential value).

In the fabric-aware extraction problem, the boundary of a motif is always an interface between two motifs. Consider an interfacial element between motif 1 and 2, and suppose it has the same local index k in both motifs. From $Q_k^{(1)} = \sum_{j=1}^{N_1} C_{kj}^{(1)} U_j^{(1)}$, we have

$$C_{kk}^{(1)} U_k^{(1)} - Q_k^{(1)} = - \sum_{j=1, j \neq k}^{N_1} C_{kj}^{(1)} U_j^{(1)}. \quad (11)$$

Similarly, for motif 2 we have

$$C_{kk}^{(2)} U_k^{(2)} - Q_k^{(2)} = - \sum_{j=1, j \neq k}^{N_2} C_{kj}^{(2)} U_j^{(2)}. \quad (12)$$

Due to the continuity of electric field, $U_k^{(1)} = U_k^{(2)} \equiv U_k$, and $Q_k^{(1)} + Q_k^{(2)} = 0$. We then derive:

$$U_k = \sum_{j=1, j \neq k}^{N_1} \frac{-C_{kj}^{(1)}}{C_{kk}^{(1)} + C_{kj}^{(2)}} U_j^{(1)} + \sum_{j=1, j \neq k}^{N_2} \frac{-C_{kj}^{(2)}}{C_{kk}^{(1)} + C_{kj}^{(2)}} U_j^{(2)}. \quad (13)$$

It is proved that the weight coefficients in (13) are a set of probabilities [11]. So, U_k can be regarded as a mathematical expectation, and calculated with a random sampling process.

With (10) and (13), a Markov-chain random walk scheme

is presented to calculate the coupling capacitances:

$$C_{ij} = Q_i = \left(-C_{ii}^{(1)}\right) \lim_{n \rightarrow \infty} \frac{n_j}{n}, \quad j \neq i, \quad (14)$$

where n is the total number of walks starting from conductor i , and n_j is the number of walks terminating at conductor j . Similarly, the total capacitance of conductor i can be calculated as [11]:

$$C_{ii} = C_{ii}^{(1)} + \left(-C_{ii}^{(1)}\right) \lim_{n \rightarrow \infty} \frac{n_i}{n}, \quad (15)$$

Compared with the FRW method, the MCRW avoids the geometry computation for constructing the transition cubes. The Monte Carlo procedure in MCRW produces sample value of either 0 or $-C_{ii}^{(1)}$, and therefore has faster convergence rate. However, the application of MCRW relies on the assumption that the whole structure is a composition of sub-structures whose BPCMs are already available.

III. MACROMODEL-AWARE RANDOM WALK ALGORITHM

In this section, we describe a new random walk method utilizing the macromodels. It is able to extract the capacitances for a general structure which is partially described by macromodels. We then discuss how to use it in order to extend and improve the FRW based capacitance extraction.

A. The Random Walk Scheme with Patch Regions

The idea is to connect the MCRW for a sub-structure with macromodel and the FRW for the structure elsewhere, through a blank patch region. As shown in Fig. 3, with a patch region touching the sub-structure's boundary, this part of boundary can be regarded as the interface of two motifs. Thus, the MCRW scheme (14) becomes possible for calculating the potential on the sub-structure's boundary, providing the macromodel for the patch region is available. Once the current position of random walk is outside the sub-structure, the FRW procedure can be employed. In Fig. 3, blue dashed-line boxes stand for the patch regions, dashed-line arrow and solid-line arrow represent a MCRW hop and a FRW hop, respectively.

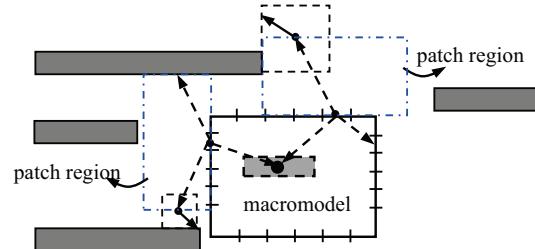


Fig. 3: With a patch region, the walk can jump out of the macromodel of sub-structure, and then behaves as a floating random walk.

Because the patch region is a conductor-free space, it is suitable for sub-structures surrounded by arbitrary environment. Another property of such patch region is that its BPCM changes little if the region is scaled in size. In Fig. 4, we show two blank regions with same shape, but with different sizes. Suppose the boundary discretization of one is the scaled version of the other's discretization, each including N boundary elements. The BPCMs of the two regions fulfill:

$$\frac{1}{l'} \mathcal{C}' = \frac{1}{l} \mathcal{C}, \quad (16)$$

where l and l' are the lengths of two blank regions, respectively. This relationship can be derived from (8), or the physical meaning of BPCM. Therefore, we only need

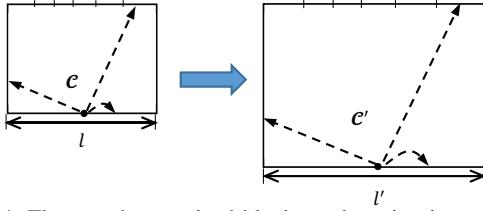


Fig. 4: The pre-characterized blank patch region is scalable.

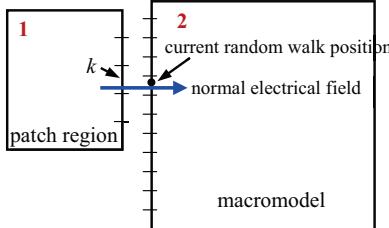


Fig. 5: Mismatched discretizations at the interface between a patch region and the macromodel sub-structure. The interface is intentionally spitted to deliver a clear view.

to pre-calculate the BPCM for one blank region, and the scaled instances of it can be used as patch regions without macromodeling cost. As shown in Fig. 3, we scale the region to become as large as possible to touch the nearest conductor.

For the shape of the patch region, half of a cube is a good choice. When the random walk stops at the boundary of sub-structure, a conductor-free cube centered at the current position can be constructed and its half outside the sub-structure is regarded as the patch region. This strategy has two advantages: 1) It makes easy to find the largest patch region touching a nearby conductor, because that is similar to finding the largest transition cube in FRW procedure, and the space management techniques [13] can be used. 2) Because the current random walk position always corresponds to same local boundary element in the patch region's macromodel, from (13) we find out that only one row of the BPCM is useful. So, the memory overhead for presenting the patch region is marginal.

Different from the MCRW in [11], our method does not guarantee that the boundary discretization meshes of the sub-structure and patch region match at their interface. Therefore, Eq. (13) cannot be directly employed. To handle this issue (see Fig. 5), the formula for MCRW should be modified. Notice that Eqs (11) and (12) still hold. Due to the continuity of normal electric field intensity, we have:

$$\frac{Q_k^{(1)}}{A_k^{(1)}} + \frac{Q_k^{(2)}}{A_k^{(2)}} = 0, \quad (17)$$

where $A_k^{(1)}$ and $A_k^{(2)}$ are the areas of the k -th boundary elements of regions 1 and 2 respectively.

With (11), (12), and (17), we have:

$$U_k \frac{C_{kk}^{(1)}}{A_k^{(1)}} + U_k \frac{C_{kk}^{(2)}}{A_k^{(2)}} = - \sum_{j=1, j \neq k}^{N_1} \frac{C_{kj}^{(1)}}{A_k^{(1)}} U_j^{(1)} - \sum_{j=1, j \neq k}^{N_2} \frac{C_{kj}^{(2)}}{A_k^{(2)}} U_j^{(2)}, \quad (18)$$

So,

$$U_k = \sum_{j=1, j \neq k}^{N_1} \frac{-C_{kj}^{(1)}}{\frac{C_{kk}^{(1)}}{A_k^{(1)}} + \frac{C_{kk}^{(2)}}{A_k^{(2)}}} U_j^{(1)} + \sum_{j=1, j \neq k}^{N_2} \frac{-C_{kj}^{(2)}}{\frac{C_{kk}^{(1)}}{A_k^{(1)}} + \frac{C_{kk}^{(2)}}{A_k^{(2)}}} U_j^{(2)} \quad (19)$$

It can be proved that each coefficient in front of U items in (19) is positive, and the sum of these coefficients equals to 1.

So, Eq. (19) suggests a new MCRW scheme for the situation with mismatched interface discretization.

B. Algorithm Description and More Details

The macromodel-aware random walk algorithm is presented in Algorithm 1. It considers the situation where there are more than one sub-structures described by macromodels. And, the capacitances of a normal outside conductor or those of a conductor within the sub-structure can be extracted.

Algorithm 1 The macromodel-aware random walk algorithm

```

1: Load the pre-calculated transition probabilities and weight values
   for the unit-size cubic transition domain;
2: Load a row of the BPCM for the half-cube patch region;
3: Generate or load BPCMs for specified sub-structures;
4: if the master conductor  $i$  is not within a sub-structure then
5:   Construct the Gaussian surface enclosing conductor  $i$ ;
6: end if
7:  $C_{ij} := 0, \forall j; npath := 0;$ 
8: repeat
9:    $npath := npath + 1;$ 
10:  if conductor  $i$  is not within a sub-structure then
11:    Randomly pick a point  $r$  on the Gaussian surface, and
        generate a cubic transition domain centered at  $r$ ; pick a
        point  $r^{(1)}$  on the domain's surface  $S$  with the transition
        probabilities;
12:     $\omega := \omega(r, r^{(1)})$  in (2);
13:  else
14:    Make a MCRW hop to point  $r$  according to (10), using
        BPCM for the sub-structure containing conductor  $i$ ;
15:     $\omega := -C_{ii}^{(1)}$  in (10)
16:  end if
17:  while current random walk position  $r_x$  is not on a conductor
   do
18:    if  $r_x$  is outside of any sub-structure then
19:      Construct the transition cube taking sub-structures as
         obstacles, and make a FRW hop to  $r_y$ ;
20:    else if  $r_x$  is at the interface of two sub-structures then
21:      Make a MCRW hop to  $r_y$  according to (13);
22:    else
23:      Construct a blank half-cube patch region and make a
         new random walk hop to  $r_y$  according to (19);
24:    end if
25:     $r_x := r_y$ ;
26:  end while
27:   $C_{ij} := C_{ij} + \omega; //the current point is on conductor j$ 
28: until the convergence criterion is met
29:  $C_{ij} := C_{ij}/npath, \forall j \neq i; //j includes the infinite ground$ 
30:  $C_{ii} := -\sum_{j \neq i} C_{ij} .$ 

```

In Step 19 of Algorithm 1, the sub-structures with macromodels are considered as obstacles for constructing the largest FRW transition cube. So, for problem with many conductors where the space management [13] is employed, we insert the bounding-boxes of sub-structures into the space management structure. Step 23 corresponds to the situation when the current position r_x is on the outer boundary of sub-structure. The half-cube patch region is got by first constructing the largest transition cube centered at r_x without taking r_x 's owner sub-structure as an obstacle, and then taking the half of cube outside the sub-structure. For constructing this transition cube we shall inquire the second nearest distance from the space management structure. A little modification to the techniques in [13] has been made in this work to support this request.

It should be pointed out, to make a feasible MCRW hop, we must guarantee that each BPCM [i.e. \mathcal{C} 's in (11), (14) and (20)] has positive diagonal and nonpositive off-diagonal entries, and the sum of each row equals to one.

The algorithm is also compatible to the techniques for multi-dielectric problem. For the blank patch regions including various dielectric configurations, a pre-characterization procedure should be employed to calculate the corresponding BPCM rows. Like the technique in [12], we can enumerate the configurations of two-layer dielectrics for the blank patch region, and then calculate the BPCM row for each configuration. While extracting a multi-dielectric structure, the pre-characterized BPCM rows are first loaded, and then the patch region including at most two dielectric layers is used during the random walk procedure. For building the macromodel for a multi-dielectric sub-structure, the technique in [8] works.

C. Application to Capacitance Extraction Problems

1) Encryption of Sensitive Structure: To hide the structure information of sensitive device or IP block, the foundry or IP vendor can choose a region and build the macromodel for it. This region is presented to EDA vendor or IC designer as a black box (see Fig. 6), represented by the macromodel instead of detailed geometry and material information.

The macromodel mainly includes the BPCM matrix, and the dimensions of the whole black box. The coordinates for the outer boundary elements of the region and the indices in BPCM standing for inside conductors should also be included. BPCM is usually a dense square matrix, and is definitely symmetric. Since the quantity and size of such black-box regions are not large, the memory cost brought to the macromodel-aware random walk algorithm is acceptable.

2) Handling Complicated Sub-Structure: To extend the ability of FRW method for handling complex IC structures (like non-Manhattan metal, conformal dielectric, etc.), we can build macromodels for sub-structures enveloping the individual structure features so that the outside geometry is of Manhattan shapes resided in planar dielectrics. E.g., the sub-structure can be the one enclosing the local region of conductors under conformal dielectric, as shown in Fig. 7. The majority of a VLSI layout is of Manhattan shapes in multi-layered dielectrics, and a small quantity of sub-structures are often enough to cover the complex structure features. So, the time cost for building macromodels is amortized. With this approach, we can extract the capacitances accurately while preserving the high efficiency of FRW method for very large layout.

3) Problem with Repeated Layout Patterns: The repeated (or cyclic) standard cells occur in the layout of memory IC or

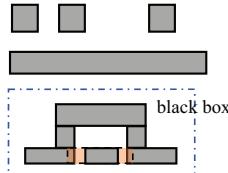


Fig. 6: With macromodel, a sensitive FinFET structure can be encrypted as a black box during the extraction.

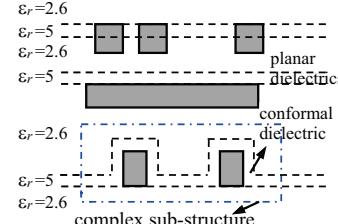


Fig. 7: The cross-section view of a structure including conformal dielectric.

FPGA. However, the upper-level interconnects above them do not exhibit the cyclic property. So, it is impossible to treat the whole structure as a composition of some small sub-structures like [11]. To take advantage of the vast repeated layout pattern, one can build a macromodel for a pattern, and then extract the capacitances with the proposed Algorithm 1. This brings several benefits: 1) the memory cost for storing layout may be reduced; 2) Because the sequence of sampling values from the MCRW procedure has less variance (see Step 15 in Algorithm 1), and MCRW is mostly executed, the capacitance extraction can be accelerated. This is similar to the high performance shown in [11] for the fabric-aware extraction problem.

Besides, for the structures in fabric-aware extraction problem [11], the empty motifs to mimic infinity boundary conditions are unnecessary if employing the proposed algorithm. This may further improve the accuracy and efficiency.

IV. NUMERICAL RESULTS

The presented techniques have been implemented in C++. 3-D structures are constructed to demonstrate the usage and efficiency of the proposed macromodel-aware random walk algorithm. The termination criterion for all random walk based algorithms is set to 0.5% 1- σ error. All results are obtained from the execution of serial computing on a Linux server with Intel Xeon 2.0GHz CPU. The test cases are as follows.

Case 1: A FinFET structure shown in Fig. 6. The minimum width of metals in black box is 20nm. Above that there are 3×3 crossover wires, each with width 50nm and height 100nm.

Case 2: A larger FinFET structure, similar to Case 1, but including two FinFET black boxes.

Case 3: A structure including conformal dielectric as shown in Fig. 7. Seven dielectrics have relative permittivities 2.6 and 5 alternately, from bottom to top. The width is 30nm for bottom-level wires, and 50nm for upper-level wires.

Case 4: A structure including a 45°-angle bevel wire at M3 layer, above a 3×3 crossover at M1/M2 layers (see Fig. 8). Metal widths are 100nm, 50nm, and 50nm, respectively.

Case 5: A structure with cyclic sub-structure like that in Fig. 9. M1 wires have width 20nm and height 30nm, while M2 and M3 wires have width 50nm and height 80nm. The layout of M1 is 8×8 duplication of a 4-metal-block pattern.

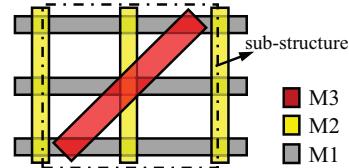


Fig. 8: A structure with a 45°-angle bevel wire (Case 4).

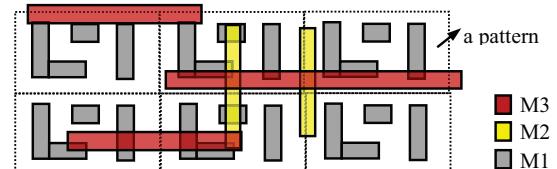


Fig. 9: A structure with 3 metal layers, where the layout of M1 is a 2×3 cyclic placement of a pattern.

In Case 1 and 2, the sub-structure selected for encryption is shown in Fig. 7. Its macromodel (BPCM matrix) is provided as input data. For Case 3 and 4, the macromodels are built

for sub-structures containing the conformal-dielectric region or the bevel wire region respectively (see Fig. 8 and 9). For the last case, a macromodel is built for the M1 pattern structure. Except for Case 3, the single-dielectric environment with $\varepsilon_r = 1$ is assumed. For Case 3, the approach in [12] has been implemented, with multi-dielectric GFTs and WVTs generated by the TechGFT program [16]. The blank patch region has been pre-characterized under a dense discretization. The corresponding BPCM row costs 162KB for single-dielectric cases, or 1.5MB for the multi-dielectric case.

The capacitances of a wire in the middle metal layer is extracted for each case using the algorithm presented in this paper. The computational results, along with those obtained from the FRW solver RWCap2 [16] or Raphael [3], are listed in Table I. Because RWCap2 is not able to handle Case 3 and 4, Raphael RC3 is run for comparison. Raphael runs very slowly and is only for accuracy validation. From the results, we see that the proposed method using macromodels exhibits good accuracy. The slightly larger error for Case 3 may be caused by different outer-boundary condition assumed in Raphael RC3. They validate the ability and efficiency of the proposed technique for handling encrypted or complex structures. And, with the new macromodel-aware random walk scheme both the number of random walk (N_{walk}) and the average number of hops (N_{hop}) are reduced, bringing up to **2.1X** speedup.

TABLE I: The results of proposed algorithm and RWCap2 (or Raphael) for the test cases.

Test	RWCap2 or Raphael	The proposed method								
Case	N_{walk}	N_{hop}	C(aF)	Time	N_{walk}	N_{hop}	C(aF)	Err(%)	Time	Sp.
1	351K	39.5	21.39	3.27	292K	30.8	21.6	1.0	1.97	1.7
2	161K	37.4	21.86	1.47	125K	26.5	22.06	0.9	0.71	2.1
3	–	–	66.14	–	370K	39.2	67.23	1.6	3.86	–
4	–	–	47.68	–	152K	20.0	48.00	0.7	0.72	–
5	217K	27.7	43.31	1.63	175K	20.0	43.60	0.7	0.94	1.7

The relevant data for building the BEM macromodels are listed in Table II. From it we see that for most cases the macromodel can be built within a couple of seconds, with less than 10MB data size. In Case 4, the 45° -angle bevel wire has larger dimensions so that it needs a larger-size macromodel. It should be pointed out, the time in Table I is for extracting only one master conductor. For extracting the whole capacitance matrix, the time overhead of building macromodels can be largely amortized.

TABLE II: The runtime for building the macromodels and their data size (Time in unit of second).

Sub-structure	Property	#element	Time(s)	Size
FinFET (Case 1/2)	7 conductors	1200	4.2	8.2MB
conformal (Case 3)	multi-dielectric	1332	2.87	7.1MB
bevel wire (Case 4)	45° -angle wire	3774	24.1	45MB
cyclic pattern (Case 5)	4 conductors	1264	2.70	6.4MB

TABLE III: The results of extracting the capacitances of a conductor within the repeated layout pattern (Time in unit of second).

Test	RWCap2	The proposed method								
Case	N_{walk}	N_{hop}	C(aF)	Time	N_{walk}	N_{hop}	C(aF)	Err(%)	Time	Sp.
5(1)	577K	14.1	5.807	2.13	8K	10.2	5.884	1.3	0.18	12
5(2)	286K	35.2	3.719	2.75	16K	18.5	3.747	0.8	0.44	6

Experiments on extracting the capacitances of conductors within a macromodel are also carried out for the structure with cyclic patterns. For Case 5, two conductors in a sub-structure are set as the master conductors individually. The results obtained from the proposed method and RWCap2 are listed in Table III. We see that the proposed algorithm largely reduces N_{walk} . It causes more than **10X** speedup over RWCap2. This validates the high efficiency brought by the MCRW process.

V. CONCLUSIONS

Experiment results have demonstrated that our algorithm extends the capability of FRW based capacitance extraction for handling structures with encrypted sensitive sub-structures and complex geometry features, and accelerates the extraction of structure with cyclic patterns as well. It exhibits good accuracy and negligible overhead, while bringing more than **10X** speedup over the fast FRW capacitance solver in some scenarios.

ACKNOWLEDGMENT

This work is supported by National Natural Science Foundation of China under Grant No. 61422402.

REFERENCES

- [1] A. N. Bhoj, R. V. Joshi, and N. K. Jha, “3-D-TCAD-based parasitic capacitance extraction for emerging multigate devices and circuits,” *IEEE Trans. VLSI*, vol. 21, no. 11, pp. 2094–2105, 2013.
- [2] W. Yu and X. Wang, *Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits*. Springer, 2014.
- [3] Synopsys Inc., “Raphael 2D, 3D resistance, capacitance and inductance extraction tool.” <http://www.synopsys.com/Tools/TCAD>.
- [4] G. Chen, H. Zhu, T. Cui, Z. Chen, X. Zeng, and W. Cai, “ParAFEMCap: A parallel adaptive finite-element method for 3-D VLSI interconnect capacitance extraction,” *IEEE Trans. Microwave Theory Tech.*, vol. 60, no. 2, pp. 218–231, 2012.
- [5] Y. Zhou, Z. Li, and W. Shi, “Fast capacitance extraction in multilayer, conformal and embedded dielectric using hybrid boundary element method,” in *Proc. DAC*, 2007, pp. 835–840.
- [6] W. Yu and Z. Wang, “Enhanced QMM-BEM solver for three-dimensional multiple-dielectric capacitance extraction within the finite domain,” *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 2, pp. 560–566, 2004.
- [7] E. A. Dengi and R. A. Rohrer, “Boundary element method macromodels for 2-D hierarchical capacitance extraction,” in *Proc. DAC*, 1998, pp. 218–223.
- [8] T. Lu, Z. Wang, and W. Yu, “Hierarchical block boundary-element method (HBBEM): a fast field solver for 3-D capacitance extraction,” *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 1, pp. 10–19, 2004.
- [9] Y. Le Coz and R. B. Iverson, “A stochastic algorithm for high speed capacitance extraction in integrated circuits,” *Solid-State Electronics*, vol. 35, no. 7, pp. 1005–1012, 1992.
- [10] K. Zhai, W. Yu, and H. Zhuang, “Gpu-friendly floating random walk algorithm for capacitance extraction of vlsi interconnects,” in *Proc. DATE*, 2013, pp. 1661–1666.
- [11] T. El-Moselhy, I. M. Elfadel, and L. Daniel, “A markov chain based hierarchical algorithm for fabric-aware capacitance extraction,” *IEEE Trans. Advanced Packaging*, vol. 33, no. 4, pp. 818–827, 2010.
- [12] W. Yu, H. Zhuang, C. Zhang, G. Hu, and Z. Liu, “RWCap: A floating random walk solver for 3-D capacitance extraction of very-large-scale integration interconnects,” *IEEE Trans. Computer-Aided Design*, vol. 32, no. 3, pp. 353–366, 2013.
- [13] C. Zhang and W. Yu, “Efficient space management techniques for large-scale interconnect capacitance extraction with floating random walks,” *IEEE Trans. Computer-Aided Design*, vol. 32, no. 10, pp. 1633–1637, 2013.
- [14] G. Rollins., “Rapid3D 20X performance improvement, Online presentation,” 2010, <http://www.synopsys.com/Community/UniversityProgram/Pages/Presentations.aspx>.
- [15] W. Shi and W. Qiu, “Encrypted profiles for parasitic extraction,” US patent No. US8499263B1. Jul. 2013.
- [16] <http://learn.tsinghua.edu.cn:8080/2003990088/rwcap.htm>.