Low Power Passive Equalizer Optimization Using Tritonic Step Response

Ling Zhang[1], Wenjian Yu[2], Haikun Zhu[1], Alina Deutsch[3],
George A. Katopis[4], Daniel M. Dreps[5], Ernest Kuh[6], Chung-Kuan Cheng[1]

[1]Univ. of California, San Diego, CA [2]Tsinghua University, Beijing
[3]IBM T.J.Watson Research Center, Yorktown Heights, NY [4]IBM System Group, Poughkeepsie, NY
[5] IBM System and Technology Group, Austin, TX [6]Univ. of California, Berkeley, CA
[1]{lizhang,hazhu,ckcheng}@cs.ucsd.edu, [2]yu-wj@tsinghua.edu.cn
[3,4,5]{deutsch,katopis,drepsdm}@us.ibm.com, [6]kuh@eecs.berkeley.edu

ABSTRACT

A low power passive equalizer using RL terminator is proposed and optimized in this work. The equalizer includes an inductor in series with the resistive terminator, which boosts high frequency components and therefore improves the interconnect bandwidth with little overhead on power consumption. An analytic estimation method for eye-opening and jitter based on tritonic step response is also introduced in this work, which enables the optimization procedure. Our experimental results show that our estimation method is accurate and a board level transmission line of 50cm wire length can achieve 15Gb/s data rate. With 15GHz frequency input, the power consumption of the equalizer is less than 2.5mW, and the total power is 5mW.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: Integrated Circuit–Design Aid

General Terms

design performance

Keywords

transmission line, equalizer, low power

1. INTRODUCTION

In the past few years, it has been demonstrated that very high data-rates in the order of tens of Gbps can be achieved using simple resistive termination for system-level interconnects [5],[6],[3]. To fully utilize the high performance that can be generated on chip, it is important to improve the performance of package-level interconnects so that the entire digital system can work at higher frequencies. The control of the signaling power, however, is becoming an ever greater challenge since many approaches that improve performance also increase the system power and therefore a low power signaling scheme is needed.

As an important approach to reducing the inter-symbol interference (ISI), various equalization schemes have been widely used. In 1920's, the concept of equalization was introduced in ([1],[2]). In [9], a constant-R ladder network was described, which can also be used as a equalizer.

More recently, [13] proposed an adaptive passive equalizer based on a RLC T-junction network with tunable resistance parameter. It claims better power efficiency than active equalizer, and experimental results showed 32mW power consumption when working at 10GHz frequency.

In this paper, we propose a very simple and effective passive equalizer for package to board level interconnect: RL terminator (Fig. 1). The idea of adopting inductance at the front end of receiver is very straight forward. Due to the low pass characteristic of transmission line, high frequency components in the input signals have a much larger attenuation than low frequency components, which causes ISI and limits the communication bandwidth. Inductance at the receiver end has a very high impedance for high frequency components, making the termination close to an open circuit and therefore boosts the magnitude of high frequency components, or in other words, "equalizes" the magnitude of different frequency components. By doing so, the ISI is alleviated and the interconnect performance is improved.

To assess the quality of the received signal, evaluation of typical eye-diagram is used. Pseudo-random bit sequence (PRBS) with length of thousands of bits is used to generate eye-diagram, which is very time consuming. Moreover, in many cases, simulation of the eye-diagram provides little insight for the optimization tasks.

In contrast, it is convenient to obtain the simulated step response. The step response contains all the necessary information for characterizing the eye, because superposition holds for Linear-Time-Invariant (LTI) system. In [14], a predictive model for evaluation of eye-opening and jitter based on bitonic step response has been proposed. We develop a more general model which is based on tritonic step response for the same purpose, and with the aid of such a simple estimation tool we perform optimization for the RL terminator.

Our main contribution includes the following:(1) a passive equalizer of RL terminator; (2) an analytic estimation of eye-opening and jitter based on step response; (3) an optimization flow using Sequential Quadratic Programming(SQP).

Our experimental results indicate that the 50cm transmission line can achieve 15Gb/s data rate by using RL termina-

DAC 2008, June 8–13, 2008, Anaheim, California, USA

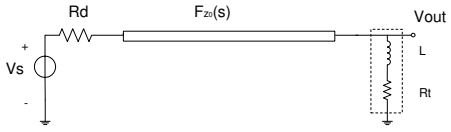


Figure 1: Transmission line with RL terminator

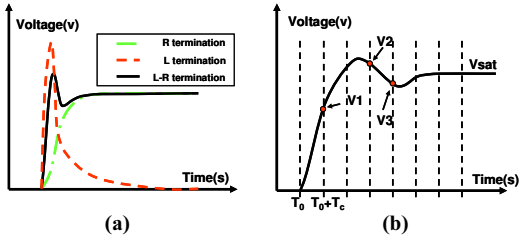


Figure 2: (a): step responses with different terminations, (b): a generic tritonic step response

tor, and the equalizer consumes power of less than 2.5mW.

2. RL TERMINATOR

2.1 Structure of RL terminator

The structure of the RL terminator is depicted in Fig. 1. Assuming the characteristic impedance of the line is Z_0, a matched resistor R_d is used to connect the line to the voltage source V_s. At the far end of the line, a resistor R_t with an inductor L in series serves as a terminator.

For a given transmission line, if we assume its transfer function under the condition of matching is $F_{z_0}(s)$, and $\mathcal{L}^{-1}(F_{z_0}(s)) = f_{z_0}(t)$ ($\mathcal{L}^{-1}$ is the inverse Laplace transform operation), then with a step input, the voltage at matched output port is

$$V_{out\_z_0} = \frac{1}{s} F_{z_0}(s) \tag{1}$$

If instead of a matched load, a RL load is added, the output voltage becomes

$$V_{out} = \frac{1}{s} F_{z_0}(s) \frac{2(R_t + sL)}{R_t + sL + Z_0} \tag{2}$$

Correspondingly in time domain we have:

$$v_{out}(t) = u(t) * f_{z_0}(t) * \mathcal{L}^{-1}\left(\frac{2(R_t + sL)}{R_t + sL + Z_0}\right) \tag{3}$$

in which the voltage includes reflection. The resistance and conductance of the line are frequency dependent, which make the function $F_{z_0}(s)$ very complex, and when transient time response is concerned, there is no closed form solution for $f_{z_0}(t)$.

2.2 Definition of tritonic step response

Three illustrative step responses with different termination conditions are shown in Fig 2(a). With pure resistive termination, the output waveform slowly rises up and monotonically reaches saturation voltage level, while with pure inductive termination, the output has a sharp rising edge at the beginning and then slowly falls back to zero. With RL termination, the response is something in between of the first two. It rises quickly, due to the effect of inductor at high frequency, and then falls down as the inductive effect diminishes and more low frequency components come in. When more current flows through the resistor, DC output voltage increases and the output rises as if terminated by a pure resistor.

With RL termination, the step response falls into one of the following three categories.

(1) Monotonic step response: the step response monotonically increases to its saturation voltage.

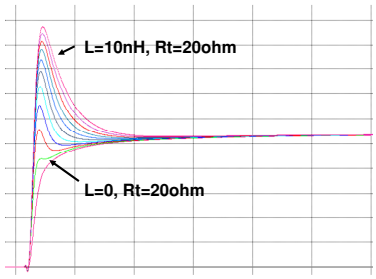


Figure 3: Step responses of $Rt = 20\Omega$, $0 \leq L \leq 10$nH

(2) Bitonic step response: the step response monotonically increases to its peak voltage and then monotonically decreases to its saturation voltage.

(3) Tritonic step response: the step response monotonically increases to its local maximal voltage, and then monotonically decreases to its local minimal voltage, and finally monotonically increases to its saturation voltage.

For simplicity, we define the above three types of step responses as *tritonic step response*. A generic tritonic step response is shown in Fig. 2(b), where T_0 is the rise time of the output node, T_c is the cycle time.

Because eye diagram is derived by folding transient response with T_c, only the voltages at integral boundaries of T_c from T_0 are of interest. These voltages form a discrete voltage array V_i: the voltage at $T_i = T_0 + iT_c, i = 0, 1, 2, ...$ We characterize the generic tritonic step response with 4 pivotal points in V_i:

(1) V_1: the voltage at $T_1 = T_0 + T_c$.
(2) V_2: the local maximum of V_i.
(3) V_3: the local minimum of V_i.
(4) V_{sat}: final saturation voltage of V_i.

For monotonic step response, $V_2 = V_3 = V_{sat}$, while for bitonic step response, $V_3 = V_{sat}$. For simplicity, we further define t_2 as the time of V_2, and t_3 as the time of V_3.

2.3 The effect of L, R value upon the step response

First of all, R_t value determines the saturation voltage. Since larger R_t results in larger reflection, V_1 increases due to the sharper rising edge. From Fig. 3, it is observed that larger L gives larger V_{peak}, and also larger V_1. The relationship between V_2 and L, R magnitude is more subtle. When L is small, V_{peak} is not large, and the waveform falls quickly from the peak value, resulting in a V_2 smaller than V_{sat}. When L is large, V_{peak} is high and it takes much longer time for voltage to drop. Before it drops below V_{sat}, the R effect has made the voltage saturate, which means V_2 equals V_{sat}.

In summary, V_{sat} is determined by R_t, larger R_t and L introduce larger V_{peak} and V_1, while V_2 relies more on the relative magnitude of L compared to R_t. Consequently, there exists a certain R_t and L values that generate larger eye-opening and smaller jitter.

3. ANALYTIC ESTIMATION FOR THE EYE-OPENING AND JITTER

The eye diagram is generated by cutting the transient response into pieces of multiple cycles and then folding them together. The transient response is derived by superimposing the step responses with weights of $+1$ or -1, according to the input PRBS pattern. Therefore the step response contains all the necessary information for estimating the quality of the eye. In this Section, we briefly discuss our simple analytic method for eye-opening and jitter estimation. For conciseness, we show the correctness pictorially and omit the proof.

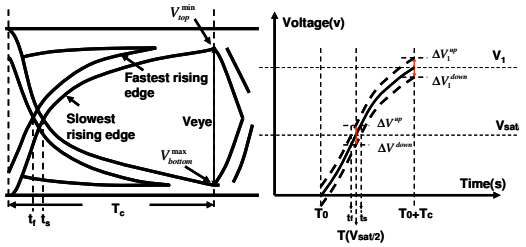


Figure 4: (a): A qualitative view of eye-diagram, (b) Relation between jitter and voltage variation on V_1

3.1 Analytic estimation for eye-opening

A qualitative view of eye-diagram is depicted in Fig. 4(a). To estimate the eye-opening, we need to know the minimum voltage a rising edge can get to at multiples of cycle time, denoted as V_{top}^{min}, and the maximum voltage a falling edge can get to at multiples of cycle time, denoted as V_{bottom}^{max}. Eye opening is $V_{eye} = V_{top}^{min} - V_{bottom}^{max}$.

Theorem 1: $V_{top}^{min} = V_1 + V_3 - V_2$ for tritonic step responses.

Lemma 1: $V_1 + V_3 - V_2$ is an achievable rising edge voltage.

Lemma 2: $V_1 + V_3 - V_2$ is the lower bound of rising edge voltage.

Regarding to V_{bottom}^{max}, we have the following two lemmas.

Lemma 3: $V_{sat} + V_2 - V_3 - V_1$ is an achievable falling edge voltage.

Lemma 4: $V_{sat} + V_2 - V_3 - V_1$ is the upper bound of falling edge voltage.

Consequently, the worst case eye-opening for tritonic step responses is

$$V_{eye} = 2(V_1 + V_3 - V_2) - V_{sat}. \tag{4}$$

Note that Eq. 4 is also applicable to monotonic and bitonic step response too, in which cases $V_2 = V_3 = V_{sat}$ and $V_3 = V_{sat}$ respectively.

3.2 Analytic estimation for jitter

To determine the worst-case jitter, we need to find the timing difference of fastest and slowest rising edge crossing the threshold voltage $\frac{V_{sat}}{2}$. As shown in Fig 4(b), the jitter for rising edge is $(t_s - t_f)$. Since the symmetry of eye-diagram, the overall jitter equals to the rising edge jitter.

To derive the value of $(t_s - t_f)$, we assume that voltage-time curve is a linear function with a slope of k for $t_f \le t \le t_s$. The fastest/slowest rising edge deviate a $\Delta V^{up}/\Delta V^{down}$ from $\frac{V_{sat}}{2}$ at $t(V_{sat}/2)$. Thus we have the following theorem:

Theorem 2: The worst case jitter is bounded by $t_s - t_f \approx \frac{\Delta V^{up} + \Delta V^{down}}{k}$.

We also assume that the voltage fluctuation around $\frac{V_{sat}}{2}$ can be approximated by the voltage variation at V_1, which means

$$\Delta V^{up} + \Delta V^{down} \approx \Delta V_1^{up} + \Delta V_1^{down}. \tag{5}$$

We use Theorem 3 for the calculation of voltage variation at V_1.

Theorem 3: $\Delta V_1^{up} + \Delta V_1^{down} = V_{sat} + 2(V_2 - V_3) - V(T_2)$.

$V(T_2)$ is defined as the voltage at $T_2 = T_0 + 2T_c$. It is obvious that the slowest rising edge results in minimum V_{top}, and we have demonstrated in Section 3.1 that $V_{top}^{min} = V_1 + V_3 - V_2$, therefore

$$\Delta V_1^{down} = V_2 - V_3. \tag{6}$$

Next we need to show that $\Delta V_1^{up} = V_{top}^{max} - V_1 = V_{sat} - V(T_2) + V_2 - V_3$.

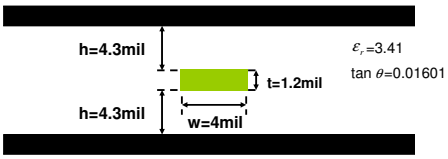


Figure 5: Cross section of the 50cm wire on board

Lemma 5: $V_{sat} - V(T_2) + V_2 - V_3 + V_1$ is an achievable rising edge.

Lemma 6: $V_{sat} - V(T_2) + V_2 - V_3 + V_1$ is the upper bound of the rising edge. It is not hard to show that Theorem 3 is also valid for monotonic and bitonic step responses.

4. SQP OPTIMIZATION FLOW

It has been discussed in Section 2.3 that optimal R_t and L values exist under the metrics of eye-opening and jitter. The simple estimation method described in Section 3 provides us a fast evaluation tool for optimizing the interconnect network. In this section, we present the method for optimizing R_t and L.

Without loss of generosity, we assume the input step is 1V, and eye-opening is no larger than 1V. We define our cost function as

$$f(R_t, L) = (1 - V_{eye})jitter \tag{7}$$

Our problem formulation can be written as

$$min \quad f(R_t, L) \tag{8}$$

$$s.t. \quad 0 \le R_t \le R_{max} \tag{9}$$

$$0 \le L \le L_{max} \tag{10}$$

The first term $(1 - V_{eye})$ is always positive, and $jitter$ is also greater than zero. To decrease the cost function, V_{eye} should be maximized and $jitter$ should be minimized.

As discussed in Section 2.1, it is hard to have closed-form solution of function $f(R_t, L)$. Thus for a given R_t and L, we run simulation to get the pivotal points that characterize eye-opening and jitter, and then we use our estimation method to predict V_{eye} and $jitter$ and calculate $f(R_t, L)$.

For such a nonlinear constrained optimization, we use Sequential Quadratic Programming(SQP) to solve it, which is the state of the art nonlinear programming method, and has been implemented in Matlab. Based on the work of [10][4][11][12], the method closely mimics Newton's method for constrained optimization. At each iteration, a quasi-Newton updating method is used to derive the approximated Hessian of the Lagrangian function, which is then used to generate a QP subproblem, whose solution is used to obtain a search direction for a line search procedure.

To avoid getting trapped in a local minimum, we perform SQP on different initial points and choose the minimum as the final solution. In Section 5.3, we will see that the optimal points obtained form different initial solutions are very close to each other.

5. EXPERIMENTAL RESULTS

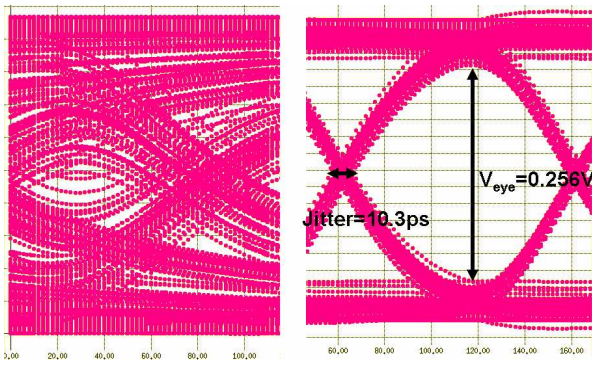
5.1 Experimental setup

We use a single-ended board level transmission line case found in memory channel for our experiments(Fig. 5). The copper wire has resistivity of ρ=1.98e-06Ωcm, and the wire length is 50cm.

We employ the 2D EM solver CZ2D from IBM [7] to extract the RLGC values of the stripline to get the frequency-dependent tabular model, and we use the IBM simulation tool

Table 1: Estimation validation at 10GHz

Cases	matched	L=3nH,R=30Ω
V_1/V_2(V)	0.241/0.483	0.309/0.316
V_3/V_{sat}(V)	0.483/0.483	0.313/0.381
V_{eye}^p(V)/$Jitter^p$(ps)	-0.003/82.8	0.251/11.2
V_{eye}^m(V)/$Jitter^m$(ps)	eye closed	0.256/10.3



(a) (b)

Figure 6: (a) Eye diagram of matching at 10GHz, (b) Eye diagram of RL termination at 10GHz

Table 2: SQP optimization results

$R_t^0(\Omega)$	L^0(nH)	$R_t^{opt}(\Omega)$	L^{opt}(nH)	CPU time(s)
30	5	39.67	6.17	3719
20	4	39.24	5.67	3338
40	6	39.68	6.21	2714
50	6	39.73	6.72	2535
60	6	39.53	6.32	3665

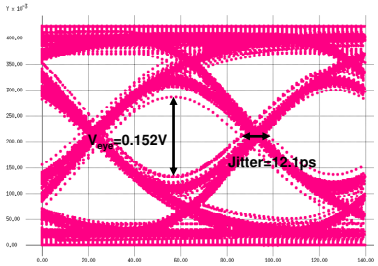


Figure 7: Eye diagram for RL termination at 15GHz, R=39.24Ω, L=5.67nH

PowerSPICE [8] to generate the step response. Then our estimation method utilizes the step response to calculate the eye-opening and jitter.

5.2 Validation of our estimation method

We use the estimation method on two simple cases(Table. 1) and compare the predicted eye-opening and jitter values with the PowerSPICE simulation results. The errors of the predicted eye-opening and jitter are 2% and 9% respectively, which is small enough for optimization purpose.

5.3 Optimization results

We use SQP flow to optimize the transmission line with RL terminator under different input data rate, and it shows that the system can support frequencies as high as 15GHz. The eye diagram is given by Fig. 7. The total power dissipation is 5mW, and the RL terminator consumes 2.48mW, in which 99.7% is burned by the resistor.

To avoid slump into local minimum, we tried five different initial solutions, as shown in Table 2. R_t^0 and L^0 are the initial solutions, and R_t^{opt}, L^{opt} are optimal solutions. It can be observed that these different solutions end up to optimal solutions that very similar to each other. Considering the smoothness of function $f(R_t, L)$, this result is reasonable.

6. CONCLUSION

A low power passive equalizer using RL terminator is introduced. The inductor at receiver end compensates the low pass filter characteristic of the transmission line and therefore improves the system bandwidth. An analytic estimation method for eye-opening and jitter based on tritonic step response is also developed and validated. The method gives the worst case eye-opening value, and the approximation of worst case jitter with less than 10% error. An optimization flow based on SQP is used to derive the optimal inductor and resistor value. The cost function considers both minimizing jitter and maximizing eye-opening. Our experimental results demonstrated that a board level transmission line of 50cm wire length can achieve 15Gb/s data rate. The power consumption of the equalizer is less than 2.5mW with 15GHz signal input while the total power consumption is only 5mW with 0.33pJ/bit.

7. ACKNOWLEDGEMENT

The authors would like to acknowledge the support of NSF CCF-0618163 and California MICRO Program, and the work of W. Yu was supported by the Basic Research Foundation of Tsinghua National Laboratory for Information Science and Technology (TNList).

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