CAPACITANCE EXTRACTION

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1. INTRODUCTION

Since the early 1950s, microwave circuits have evolved from discrete circuits to planar integrated circuits, then to multilayered and three-dimensional integrated circuits. With the increased circuit density, the multiconductor line in multilayered dielectric media has become the major form of the transmission line or interconnect. Multilayered routing reduces the area as well as the volume of the circuit. However, as a result, electromagnetic coupling among conductors greatly influences circuit performance. In some microwave integrated circuits, this coupling effect is utilized to construct compact circuit components, under most circumstances it is regarded as a parasitic effect that must be modeled accurately for verification of the circuit's validity and performance.

In the related field of very-large-scale integration (VLSI) circuits, electromagnetic coupling among interconnects is also becoming increasingly important. With the introduction of deep-sub-micrometer (DSM) semiconductor technologies, the on-chip interconnect wire can no longer be considered as an equipotential form of coupling. The parasitic effects introduced by the wires display a scaling behavior that differs from that of active devices such as transistors, and these effects tend to gain importance as device dimensions are reduced and circuit speed is increased. In fact, they begin to dominate some of the relevant metrics of digital integrated circuits such as speed, energy consumption, and reliability. A typical recursive design flowchart of a state-of-the-art integrated circuit (IC) is shown in Fig. 1, where a postlayout step termed *parasitic extraction* precedes *gate-level simulation*. The task of parasitic extraction is to model the electromagnetic effects of the wire with parasitic components of capacitance, resistance, and inductance, so that a more accurate circuit simulation can be performed.

With the increase in working frequency and development of silicon technologies, the discrepancy between the microwave IC and the common VLSI circuit becomes marginal. Therefore, the electromagnetic modeling and accurate extraction of the interconnect parasitics have become a subject of advanced research in both fields to date. Among the three parasitic parameters, capacitance has attracted the most attention because it greatly influences time delay, power consumption, and the signal integrity and its calculation becomes complicated under DSM technologies.

In the following sections, the fundamental theory and contemporary methodology and algorithms of capacitance extraction will be discussed.

2. PROBLEM FORMULATION

As is well known, the capacitor is a commonly used component in electric or electronic equipment. It is usually composed of two conductors insulated from each other. When charged, the two surfaces of the conductor facing each other carry equal and opposite charges Q and $-Q$, respectively (see Fig. 2). The electric potential difference between the two conductors ϕ_1–ϕ_2 is called the *voltage* of the capacitor and is always denoted by V. Experiments and theoretical analyses show that, for a capacitor, Q is always proportional to V and thus the ratio Q/V is a constant determined by the structure of the capacitor. This ratio is called the *capacitance* of the capacitor and is denoted by C: $C=(Q/V)$.

In the International System of Units (SI), the unit of capacitance is the faraday (F). It expresses the capacitance of a capacitor that has one coulomb on one of its polar planes when the potential difference is 1 V. Other commonly used units of capacitance are μF (10^{-6}F), pF (10^{-12}F), and fF (10^{-15}F).

The capacitance of some simple capacitor can be calculated easily. For example, for the parallel-plate capacitor shown in Fig. 2, we have

$$C=\frac{\varepsilon_0\varepsilon_r S}{d} \tag{1}$$

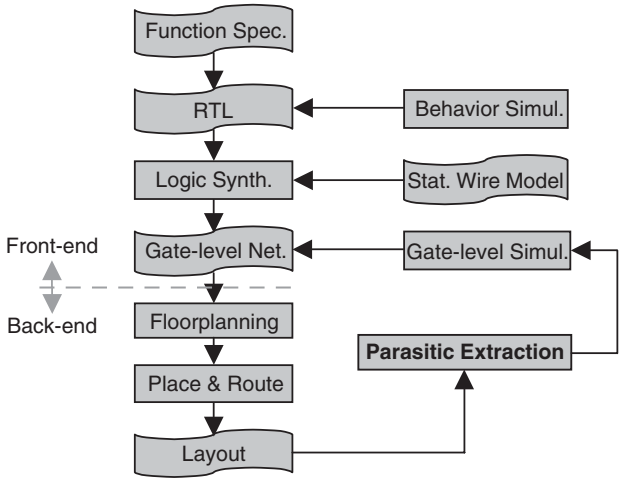

Figure 1. A typical flowchart of IC design.

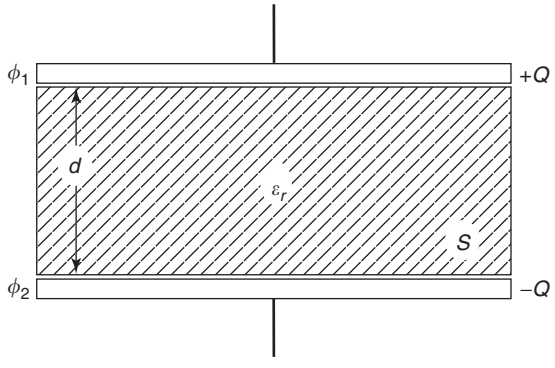

Figure 2. A parallel-plate capacitor.

where ε_0 is the dielectric constant of free space and in SI, is expressed as

$$\varepsilon_0 = \frac{1}{4\pi \times 9 \times 10^9} = 8.85 \times 10^{-12} \mathrm{C}^2/\mathrm{N} \cdot \mathrm{m}^2$$

where ε_r is the relative permittivity of the insulating material, S is the area of the plate, and d is the distance between two parallel plates.

Specific capacitors widely used in the design of microwave circuits include the interdigital capacitor and the metal–insulator–metal (MIM) capacitor. Figure 3 shows the physical layout of an interdigital capacitor with nine fingers, and Fig. 4 shows the cross-sectional view of an MIM capacitor with the GaAs process. The interdigital capacitor works with the electrostatic coupling between the intercrossed fingers, and has a very high Q value. So, it is widely used in the high-frequency microwave circuits. The MIM capacitor has simple geometry and is easily fabricated, and its capacitance is controlled by the dimensions of the polar planes. Since the interdigital capacitor and the MIM capacitor are widely used, calculation of the parameters of their structures within given the working frequency and corresponding capacitor value becomes an important issue for both design and optimization. This can be regarded as the reverse procedure of capacitance extraction. For further discussion of this issue, please refer to the literature [39,40].

Actually, the capacitor has a more generalized form than that described above; actually, it consists of two isolated conductors. The *capacitance* of a single conductor (conductor 1) is defined as if another conductor (conductor 2) were located at an infinite distance away to form a joint capacitor (conductors $1+2$). For example, the capacitance of an isolated conductor sphere with radius of R can be calculated as $C = 4\pi\varepsilon_0 R$.

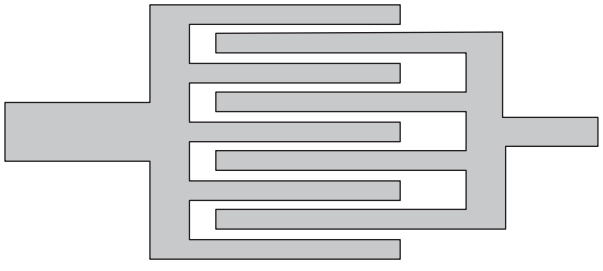

Figure 3. An interdigital capacitor.

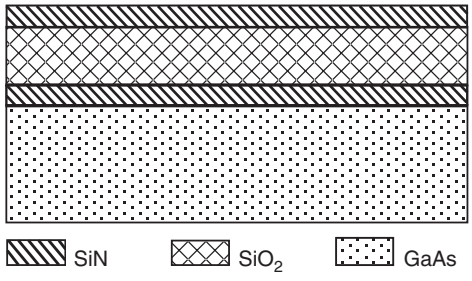

Figure 4. An MIM capacitor (cross-sectional view).

Many conductor interconnect wires are involved in the microwave IC and the common VLSI circuit, and they are insulated by some dielectric such as oxide SiO_2. The capacitance between any two wires reflects the electrostatic coupling effect between these wires, and calculating these capacitances with high accuracy is very important for analysis of the circuit's performance.

For an N-conductor system, such as the interconnect wires in an IC, an $N \times N$ capacitance matrix $[C_{ij}]_{N \times N}$ is defined by

$$Q_i = \sum_{j=1}^{N} C_{ij} U_j, \quad i = 1, 2, \ldots N, \tag{2}$$

where C_{ij} $(i \neq j)$ is the coupling capacitance between conductors i and j, and C_{ii} is the self-capacitance or total capacitance of conductor i. Q_i is the induced charge on conductor i, and U_j is the electric potential of conductor j (usually the known bias voltage).

Figure 5 shows a typical crossover wires in the VLSI system, where the coupling capacitances between any two conductors need to be calculated.

Accurate modeling of the wire capacitances in a state-of-the-art integrated circuit is not a trivial task. It is further complicated by the fact that the interconnect structure of contemporary integrated circuits is three-dimensional (see Fig. 5). The capacitance of such a wire is a function of its shape, environment, distance from the substrate, and distance to surrounding wires. Generally SiO_2 is the insulating material among interconnect wires in integrated circuits, although some materials with lower permittivity, and thus lower capacitance, are coming into use. The relative permittivity ε_r of several dielectrics commonly used in integrated circuits is presented in Table 1. It should also be pointed out that ε_r of air or vacuum is 1.

3. METHODOLOGY AND ALGORITHMS

With the advances in IC technology, the methodology of capacitance extraction has evolved from one-dimensional (1D), two-dimensional (2D), 2.5-dimensional (2.5D), to

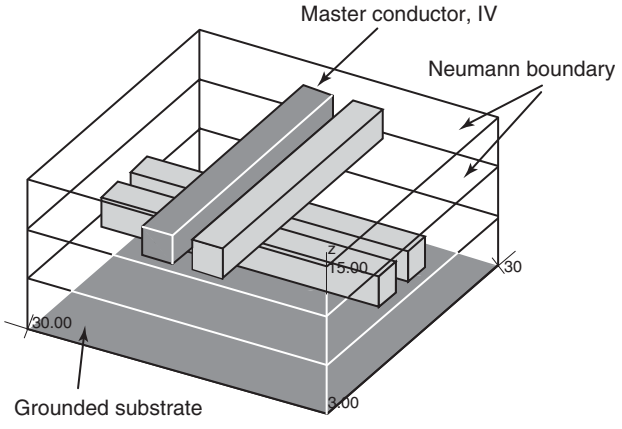

Figure 5. A structure involving 2×2 crossover interconnect wires.

Table 1. Relative Permittivity of Several Commonly used Dielectric Materials

Dielectric Material	Silicon	Alumina (Package)	Silicon Nitride (Si_3N_4)	Glassepoxy (PCB)	Silicon Dioxide	Polyimides (Organic)	Aerogels
Relative permittivity (ε_r)	11.7	9.5	7.5	5	3.9	3–4	~1.5

three-dimensional (3D) to meet the required accuracy. In this section, the 1D and 2D methods are briefly introduced. Then, the 2.5-D method and the mechanism of the modern commercial capacitance extraction tools that employ the 3D capacitance extractor are presented. Finally, we will discuss some details of algorithms of the 3D field solver for capacitance extraction.

3.1. 1D and 2D Methods

From the formula for calculation of parallel-plate capacitance [Eq. (1)], we can infer that the capacitance is proportional to the overlapping area between the conductors and inversely proportional to their separation distance. This is very important for capacitance extraction without a high degree of precision.

Figure 6 shows a typical microstrip structure, where there is only a single rectangular conductor over a ground plane. This structure is very different from the above parallel-plate model discussed because of the existence of the capacitance between the sidewalls of the wire and the substrate, called the *fringing capacitance*. To avoid the time-consuming numerical modeling of this geometry, an approximate 1D method can be used as a good engineering practice. The capacitance is assumed to be the sum of two components: (1) a parallel-plate capacitance determined by the vertical field between a wire of width w and the ground plane and (2) the fringing capacitance modeled by a cylindrical wire with radius equal to the conductor thickness H. So, this simple and practical 1D formula becomes

$$C = C_{\text{area}} + C_{\text{fringe}} = \frac{\varepsilon \cdot w}{d} + \frac{2\pi\varepsilon}{\log(d/H)}$$

where $w = W - H/2$ is a good approximation for the width of the parallel-plate capacitor (W is the width of the wire), d is the distance between the ground plane and the bottom of wire, and ε is the permittivity of the insulating material. With this formula, we obtain the approximate capacitance per unit length.

In another kind of 1D capacitance extraction, the area and perimeter parameters of interconnect geometries are first obtained. Then, a fine-tuned set of area and perimeter weights per routing layer can be used to calculate capacitance values as an inner product [1]:

$$C = (\text{area dimensions, perimeter dimensions}) \cdot (\text{area weight, perimeter weight})$$

AU:4 Such area and perimeter weights can be obtained by precharacterization of an "average" environment of a wire. The area can be that from single layer or a combination of layer overlaps.

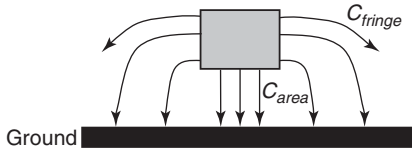

Figure 6. A conductor above a ground plane (cross-sectional view).

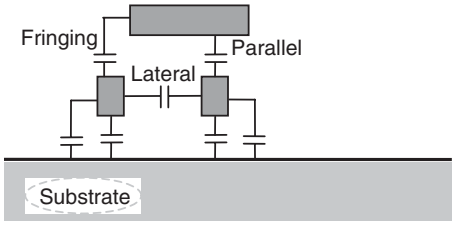

Figure 7. Capacitive coupling between wires in a multilayered interconnect system.

Usually, the 1D extraction method works well when the number of interconnect layers is restricted to only one or two. However, the current process technology often involves many more interconnect layers, and they are also of high density. So, several capacitance components of a wire embedded in the multilayered interconnect system may exist, other than the only capacitive coupling to the ground plane (see Fig. 7). Each wire is coupled not only to the grounded substrate but also to the neighboring wires on the same layer and on adjacent layers. Not all capacitive components terminate at the grounded substrate; actually a large number of them connect to other wires. These (fringing, lateral, parallel, etc.) capacitors between wires not only form a source of noise (crosstalk among signal lines) but also can have a negative impact on the circuit performance.

To model the capacitance in the multilayered interconnect system with higher accuracy, 2D capacitance extraction methodology was developed. In 2D capacitance extraction, accurate geometry modeling and numerical techniques are implemented for the cross section of simulated structure (as in Fig. 7). For the 2D region of dielectrics, the electric field equation is solved with numerical techniques. 2D extraction ignores all three dimensional details and assumes that the geometries being modeled are uniform in one dimension, usually the signal propagation direction. Therefore, 2D capacitance extraction is only suitable only for some special cases, such as like the transmission line.

The details of numerical techniques for solving the electric field will be introduced in Section 3.3, albeit in a 3D manner.

3.2. 2.5D Method and Commercial Capacitance Extraction Tool

The 2.5D (also called *qausi-3D*) method goes a step further than 2D extraction. Its main idea is to calculate the capacitance of several cross sections (using the 2D method) and combine the 2-D results into the final capacitance value.

A typical 2.5D capacitance extraction method is also called the "(2 × 2)D method", in which any 3D structure is swept in two perpendicular directions and by considering the geometry overlapping, 3D structure can be modeled more accurately (see Fig. 8).

In Fig. 8, an m_2 wire crosses an m_1 wire. Along direction A, a 2D cross-sectional view is shown in the middle. Along direction B, the other 2D cross section is shown to the right. Solving the two orthogonal strictly 2D problems numerically, we obtain $C_A = C_{1f1} + C_{10} + C_{1f2}$, $C_B = C_{2f1} + C_{20} + C_{2f2}$ (see Fig. 8). Then, $C_{m1,\,m2} = C_A \times w_1 + (C_B - C_{20}) \times w_2$, where w_1, w_2 are the widths of wires m_1 and m_2, respectively. However, this method is still not very accurate. The error could be more than 10%, especially for coupling capacitance, which is very important for signal integrity analysis.

Obviously, true 3D extraction is a straightforward method to achieve high precision. However, the 3D electrostatic Laplace equation must be solved numerically within a complicated 3D structure. This consumes extensive computational effort. 3D capacitance extraction (usually called the "field solver") is actually not a trivial extension of the 2D case. This aspect is discussed further in Section 3.3.

For the current task of capacitance extraction in modern IC design, using the 3D extraction method directly is impossible because of its huge expense of memory and CPU time. To obtain a good tradeoff between accuracy and efficiency, modern capacitance extraction tools utilize special techniques for the full-chip extraction task, which is usually divided into three major steps:

1. *Technology Precharacterization*. Given a description of the process cross sections, tens of thousands of test structures are enumerated and simulated with 2D and/or 3D field solvers. These structures are of medium dimensions. The resulting data are collected either to fit some empirical formulas or to build lookup tables (either type is called a "pattern library"). In Ref. 3, analytical equations are used for model fitting. A good fit would require fewer simulation points. The number of patterns can be reduced by pattern reduction techniques. Arora et al. [4] present a pattern compression technique that reduces the total number of precharacterizaiton patterns. With this technology, the capacitance in some layout pattern can be extrapolated from the capacitance values in two simpler precharacterization patterns, without losing much accuracy. Capacitance field solvers employ different numerical algorithms, and they may give different answers for certain special layout structures depending on the problem setup and boundary conditions. Therefore, the precharacterizaiton software should have the flexibility to incorporate any third-party field solvers. This first step should be performed only once per process technology. The challenge in this area includes the handling of increasingly complex processing technology, such as low-k dielectric, air-bubble dielectric, nonvertical conductor cross sections, conformal dielectric (see Fig. 9), and shallow trench isolations.
2. *Geometric Parameter Extraction*. This is also an integral part of precharacterization. If a geometric pattern requires 10 parameters to describe, there is a corresponding precharacterization of 1×5^{10} ($\sim$10,000,000) patterns to simulate. This is assuming that five sample points are taken in each of the 10 parameters, resulting in a 10-dimensional (10D) table of the dimensions given above. This is clearly not feasible. On the other hand, if a geometric pattern can be described by very few parameters, then it is difficult for it to be accurate. In a full-chip situation, the runtime of geometric parameter extraction can be very time/space-consuming, with millions of interconnect polygons to analyze. Time/space-efficient geometric processing algorithms are

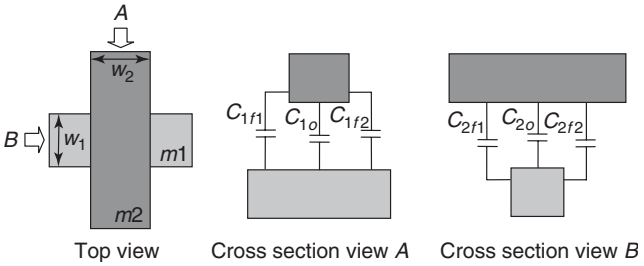

Figure 8. 2.5D capacitance for a crossover structure.

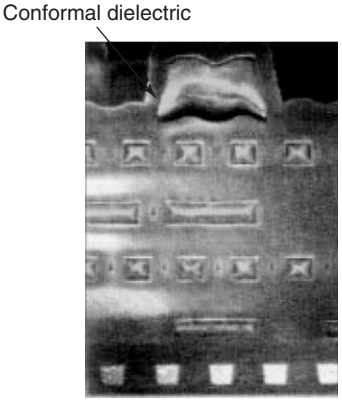

Figure 9. A realistic vertical cross section of IC interconnect. We see that conductors on layers 1–5 are trapezoidal, and there is a conformal dielectric on top of the top layer metal (passivation). (SEM photograph courtesy of IBM Corp. © Copyright IBM Corp. 1994, 1996.)

very important. Habitz and Wemple [5] present a geometric parameter reduction technique in which geometric parameters can be dramatically reduced by taking advantage of the shielding effect. Conductors two layers away from the main conductor of interest do not require a precise description. This is particularly useful for the very-deep-sub-micrometer geometry, where a very distant conductor mesh behaves like a large airplane.

3. *Calculation of Capacitance from Geometric Parameters.* Here, the geometric parameters are matched to some entries in the pattern library. Usually a full-chip or full-path extraction task involves at least thousands of conductors. The whole structure is chopped into medium-size pieces first, which are then calculated with the pattern-matching approach described above. Finally, the capacitance values must be combined to get the desired result.

One major source of error is called the *pattern mismatch*, where extracted geometry parameters do not have an exact match in the pattern library. At this time, there are two remedies to perform the capacitance calculations. One method is to enhance the pattern library by running field solvers at the full-chip extraction time. The other method is to employ heuristics to synthesize a solution from closely matched precharacterization patterns. Even if all the geometric patterns match the library completely, there could still be discontinuities in the layout pattern decomposition, which is another source of error. This error is analyzed in Ref. 6, where the error bound was obtained by utilizing the "empty" and "full" boundary conditions.

3.3. Algorithms for 3D Field Solver

The 3D method can be used model the actual geometry accurately, so it behaves with the highest precision. 3D capacitance extraction becomes increasingly important under the DSM technology of VLSI circuit, although presently it is used widely only as a library-building tool in the industry. More recently, much research work has been devoted to improve the efficiency of the 3D extraction method. Related papers are published on the annually held conferences (*Design Automation Conf.*, *Int. Conf. Computer-Aided Design*, etc.) and many academic journals (*IEEE Trans. Microwave Theory Tech.*, *IEEE Trans. Comput. Aided Design*, etc.). To date, some 3D extraction algorithms have been developed to integrate with the commercial software of some electronic design automation (EDA) companies in the Silicon Valley (in California). Research on 3D capacitance extraction is still advancing very rapidly.

In this section, the principles and mainstream techniques of the 3D field solver are introduced. More cutting-edge techniques are mentioned with related references.

3.3.1. Overview. For a system involving multiple conductors (see Fig. 5), with one conductor setting 1 V and others 0 V, the electrostatic equation (called the *Laplace equation*) need to be solved with a homogenous dielectric region [7]:

$$\nabla^2 u = \frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} + \frac{\partial^2 u}{\partial z^2} = 0 \tag{3}$$

where u is the electric potential. This equation can be transformed into different mathematical formulations. Then, various numerical methods are employed to solve it with different levels of efficiency.

According to the domain of the above Laplace equation (3), there are two models for capacitance extraction: (1) *the infinite-domain model*, in which the electrostatic field spreads to the infinite, resulting in an infinite problem space; and (2) the *finite-domain model*, where the electrostatic field is restricted within a finite domain, with the Neumann condition on the outer boundary [8]: $(\partial u/\partial n) = 0$. This means that electric field is not able to spread out of the finite problem domain. The Neumann condition is also called the *reflective boundary condition*, and is introduced as the "magnetic wall" in Ref. 9. It should be pointed out that the infinite-domain model is ideal for simulating isolated structures, but for the on-chip application it is not accurate because of the influence of neighboring conductors. On the other hand, the finite-domain model considers a part cut from actual layout of VLSI circuit; it is suitable for the realistic capacitance extraction of VLSI interconnects [8]. Now, both models of capacitance extraction are used in different applications, and accordingly the numerical methods are also different. The problems a numerical algorithm usually encountered in modeling are discussed below.

Classifications of the 3D field solver methods include the domain discretization method, the boundary integral equation method, semianalytical approaches, and the stochastic method. The domain discretization method includes the finite-difference method (FDM) [10], finite-element method (FEM) [11], and the method of the measured equation of invariance (MEI) [13,14]. The boundary integral equation method includes the method of moment [15], indirect boundary element method (BEM) [8,17–27], and direct boundary element method [28–34]. The semianalytical approaches combine the analytical formulas and some traditional numerical methods [9,35–37]. The stochastic method is based on statistical theory [38].

FDM and FEM discretize the entire 3D domain, thus producing a linear algebra system with large order; hence the computational speed of these methods is greatly limited. However, since both methods are relatively well established, they are still used in the industry as a reference tool with accurate values calculated under fine grids. For example, the famous software of $\frac{2}{3}$D capacitance extraction "Raphael" utilizes FDM, and the "SpiceLink" of Ansoft Corp. is based on FEM.

Since the mid-1990s, the boundary integral equation method has begun to replace the domain discretization method because of its high performance. In both indirect and direct BEM, only the 3D domain boundary is discretized, and a smaller system of linear equations is obtained. Problems encountered with the complex boundary can be

effectively handled with BEM, whose accuracy is superior to that of FEM as well. Thus, the BEM with rapid computating techniques has become the focus of research on the 3D field solver.

3.3.2. Indirect Boundary-Element Method. The indirect boundary method can be regarded as a variation of the method of moments (MoM). Because only the domain boundary needs to be discretized, the indirect BEM involves much fewer unknowns than does FDM or FEM. However, it leads to a dense coefficient matrix, whose formation and solution introduce many difficulties. The innovation of the multipole acceleration method, the singular-value decomposition (SVD) method, and the hierarchical method has made the indirect BEM more applicable. Now, indirect BEM combined with a fast computational technique has become a main choice for the 3D field solver.

The indirect BEM method is also called the *equivalent charge method*, whose boundary integral equation involves the surface charge density $\sigma(x')$ as an unknown function

$$u(x) = \int_{\Gamma} G(x,x')\sigma(x')da' \quad (\boldsymbol{x} \in \Gamma) \tag{4}$$

where $G(x,x')$ is Green's function. For free space, $G(x,x') = 1/||x - x'||$; Γ is the boundary surface. After solving the surface charge density $\sigma(x')$, the charge on conductor i can be calculated with

$$Q_i = \int_{S_d(i)} \sigma(x')da' \tag{5}$$

where $S_d(i)$ is the surface of conductor i. We discretize the surfaces of m conductors into n constant elements (or panels); then the potential at the center of the kth panel x_k can be expressed as a sum of the contributions of all the panels

$$u_k = \sum_{j=1}^{n} \int_{\Gamma_j} \frac{\sigma_j(x')}{\|x' - x_k\|} da'$$

where $\sigma_j(x')$ is the surface charge density of panel j (Γ_j). Substituting the known boundary conditions, we obtain a dense linear algebra equation.

$$Pq = b \tag{6}$$

where the coefficient matrix $\boldsymbol{P}$ is dense and nonsymmetric. The Krylov subspace iterative method, such as the generalized minimal residual algorithm (GMRES) [2], is usually used to solve this equation.

For a problem involving multiple dielectrics, the polarization charge density on the dielectric interface needs to be introduced, which contributes to the potential distribution together with the free charge density on conductor surfaces. Therefore, the problem becomes equivalent to that in the free space and the simple free-space Green function is used to form Eq. (4). Except for Eq. (4) on each conductor panel, the normal derivative of the potential satisfies

$$\varepsilon_a \frac{\partial u_+(x)}{\partial \boldsymbol{n}_a} = \varepsilon_b \frac{\partial u_-(x)}{\partial \boldsymbol{n}_a} \tag{7}$$

with $\boldsymbol{x} \in$ interface of ε_a and ε_b at any point $\boldsymbol{x}$ on a dielectric interface. Here $\boldsymbol{n}_a$ is the normal to the dielectric interface at $\boldsymbol{x}$ that points into dielectric a and ε_a and ε_b are the permittivities of the corresponding homogenous dielectric region; $u_+(x)$ is the potential at x approached from the side of the interface ε_a, and $u_-(x)$ is the analogous potential for the b side.

For the multidielectric problem, the so-called total-charge Green function approach presented above involves more unknowns at the interfaces. Another choice to deal with the problem is to employ the multilayered Green function. Then, only the free charge density on the conductor surfaces needs to be considered as an unknown function. However, to evaluate the Green function for the multilayered medium, infinite summations are involved, which is very time-consuming. Oh et al. [20] derived a closed-form expression of Green's function for the multilayered medium by approximating the Green function using a finite number of images in the spectral domain. This greatly reduces the computational task. Li et al. [22] presented for the first time the general analytical formulas for the static Green functions for shielded and open arbitrarily multilayered media. Zhao et al. [21] an efficient scheme for the generation of multilayered Green functions using a generalized image method presented. The multilayered Green function is much more complicated than the free-space Green function; it is applicable only to the simple stratified structure of multiple dielectrics, while for more complex structures, such as the conformal dielectric, the deduction of Green's function may be impossible.

More research work has been undertaken to accelerate the capacitance extraction using the total-charge Green's function approach. In 1991, Nabors et al. applied the multipole accelerated (MPA) method successfully, proposed earlier by Greengard and Rokhlin [16], to 3D capacitance extraction with the indirect BEM. In the MPA method, calculation of the interaction between charges [i.e., the coefficients in (6)] is divided into two parts: the near-field computation and the far-field compu-

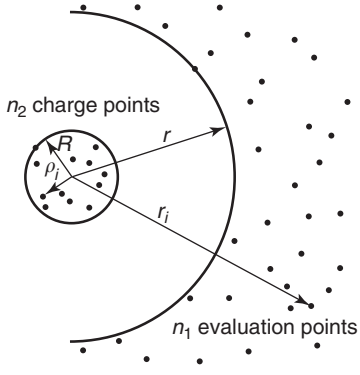

Figure 10. Evaluation point potentials are approximated with a multipole expansion [17].

tation. For the near-field computation, the coefficients are calculated directly; for the far-field computation, the multipole expansion and local expansion are used to expedite the computation. Therefore, the CPU time of forming and solving (6) with the iterative equation solver is greatly reduced. Figure 10 illustrates of the multipole expansion. Nabors and White [18], developed the adaptive, preconditioned MPA method. The corresponding software prototype FastCap is shared on the MIT Website, and has become a popular tool of capacitance extraction for relevant researchers. To date, the capacitance extraction using the MPA indirect BEM is still undergoing research [25].

In 1998, a fast hierarchical algorithm for 3D capacitance extraction was proposed at the *Design Automation Conference*, and was reprinted in a journal article [24]. Similar to the multipole algorithm, it is also based on fast computation of the "*N*-body" problem. For the singular integral kernel of $1/||x-x'||$, it can achieve high acceleration of computation, and only $O(N)$ operations are needed for each iteration. For other weaker-singular kernels, the efficiency of this method may be reduced. In 1997, Kapur et al. and Long [19] proposed an accelerated method based on the singular-value decomposition (SVD) method that is independent of the kernel and based on the Galerkin method using the pulse function as the basis function. It requires an $O(N)$ times operation to construct the coefficient matrix and $O(N\log N)$ operations to perform an iteration. The precorrected fast Fourier transform (FFT) algorithm [23] has the same computational complexity, while it is based on the collocation method for discretization.

These studies on capacitance extraction with indirect BEM all handle the infinite-domain model. In 1996, Wang et al. [8] improved the multipole accelerated indirect BEM, enabling it to handle the finite-domain problem and also proposed a parallel multipole accelerated 3D capacitance simulation method based on nonuniformed cube partition.

Other fast computational methods for indirect BEM include those based on wavelets [26] and the multiscale method [27].

3.3.3. Direct Boundary-Element Method. The direct BEM is based on the direct boundary integral equation (BIE), and is suitable for solving the 3D Laplace equation with varied boundary conditions [12]. However, the direct BEM method is generally used to deal with the finite-domain model of capacitance extraction.

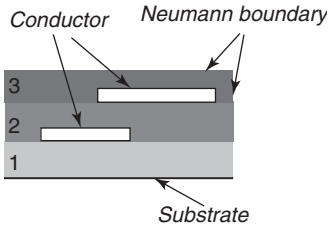

Figure 11. A structure with three dielectrics (cross-sectional view).

Within the finite domain that is involved in capacitance extraction (see Fig. 11), the electric potential u satisfies the following Laplace equation with mixed boundary conditions [32]

$$\begin{cases} \varepsilon_i \nabla^2 u = 0, & in\ \Omega_i\ (i=1,\ldots,M) \\ u = u_0, & \text{on } \Gamma_u \\ q = \partial u/\partial \boldsymbol{n} = q_0 = 0, & \text{on } \Gamma_q \end{cases} \tag{8}$$

where the whole domain $\Omega = \overset{M}{\cup}\Omega_i$, where Ω_i stands for the space possessed by the ith dielectric. Γ_u represents the Dirichlet boundary (conductor surfaces), where u is known as the bias voltages; Γ_q represents the Neumann boundary (outer boundary of the simulated region), where the electric flux q is supposed to be zero. Here $\boldsymbol{n}$ denotes the unit vector outward normal to the boundary. At the dielectric interface, the compatibility equation (7) holds.

With the fundamental solution as the weighting function, the Laplace equations in (8) are transformed into the following direct BIEs by the Green identity [12]

$$c_s u_s^i + \int_{\partial\Omega_i} q^* u^i d\Gamma = \int_{\partial\Omega_i} u^* q^i d\Gamma \quad (i=1,\ldots,M)$$

where u_s^i is the electric potential at collocation point s (in dielectric region i) and c_s is a constant dependent on the boundary geometry near to the point s. $u^* = 1/4\pi r$ is the fundamental solution of the 3D Laplace equation, whose derivative along the outward normal direction $\boldsymbol{n}$ is $q^* = \partial u^*/\partial \boldsymbol{n} = -(\boldsymbol{r},\boldsymbol{n})/4\pi r^3$, r is the distance from the collocation point to the point on Γ, and $\partial\Omega_i$ is the boundary that surrounds dielectric region i.

Employing the collocation method after discretizing the boundary, such as that in the indirect BEM, we obtain system of linear equations [32]:

$$\boldsymbol{Ax} = \boldsymbol{f} \tag{9}$$

Finally, with the preconditioned Krylov iterative equation solver, such as the GMRES algorithm [2], the normal electric field intensity on the conductor surface is obtained [32].

In direct BEM, variables of both potential and field intensity are involved; thus two kinds of integral kernels are found. Although this is more complex than the indirect BEM method, direct BEM has its own advantages: (1) it is suitable for capacitance extraction within the finite domain since two variables are included, and (2) because the variables in each BIE are within the same dielectric region, it has a "localization" characteristic, which leads to a sparse linear system for problem with multiple dielectrics.

In direct BEM, a great deal of time and memory are consumed in forming and solving the system of discretized BEM equations. Wang et al. continued the research work of Fukuda [28] on 2D capacitance extraction using direct BEM, extending it to the 3D structure of VLSI intercon-

nects [32]. An efficient analytical/semianalytical integration scheme was used to accurately calculate the boundary integrals under the VLSI planar process. This method achieves high computational speed and accuracy when forming Eq. (9) [32]. In 1996, Bachtold et al. [29] extended the multipole method to handle the "potential boundary integral" (whose kernel is $1/r^3$) in the direct BEM. They discussed the model of multiple dielectrics within the infinite domain. In 1999, Gu et al. extended the fast hierarchical method used in the indirect BEM and made it feasible to apply it for direct-BEM-based capacitance extraction [30].

In 2000, Yu et al. proposed a quasimultimedium (QMM) method, based on the localization characteristic of direct BEM [32]. The QMM method exploits the sparsity of the resulting coefficient matrix when handling the multidielectric problem. Together with the efficient equation organization and iterative solving technology, the QMM accelerated method has greatly reduced the computing time and memory usage. Figure 12 shows that a typical 3D interconnect capacitor with five dielectric layers is cut into $5 \times 3 \times 2$ fictitious medium regions. The QMM method has been successfully applied to actual 3D multidielectric capacitance extraction [32,34]. For the finite-domain multidielectric problem, the QMM-based method has shown a $10\times$ higher computation speed and memory saving over the multipole approach (FastCap 2.0) with comparable accuracy [34].

Another kind of field solver, called the "global approach," does not solve the resulting linear system in the usual way. The global approach discretizes the field equations and converts them to a circuit network of resistors or capacitors. Finally, with circuit reduction or matrix computation, the whole resistance or capacitance matrix can be obtained directly. In 1997, Dengi of Carnegie Mellon University proposed a global approach (called "macromodel" method) for 2D interconnect capacitance extraction based on direct BEM [31]. More recently, Lu et al. successfully extended the concept of boundary element macromodel to the 3D case, and developed a rapid hierarchical block boundary element method (HBBEM) for interconnect capacitance extraction [33].

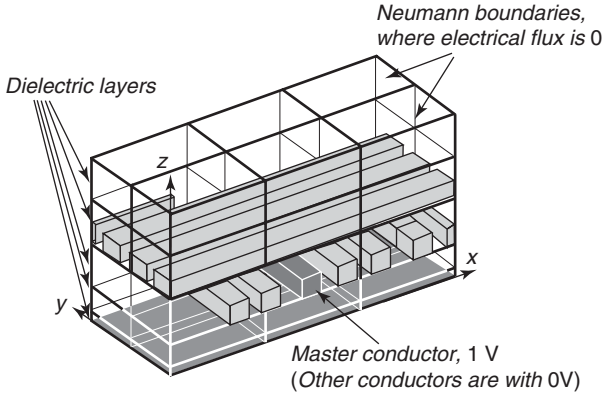

Figure 12. A typical 3D interconnect capacitor with five dielectric layers is cut into 3×2 structure.

3.3.4. Semianalytical Approaches. Semianalytical approaches have been proposed as a solution for 3D capacitance extraction. Basically, they take certain special procedures and reduce the original problem by one dimension, such as using domain decomposition. Since some subdomains with specific geometry symmetry can be handled using the analytical formula, these approaches have very high computational speed as well as much less memory usage. Another characteristic of these approaches is that the FDM is often used for the general and complicated subdomain. That is why these approaches are sometimes considered as improvements over the finite-difference method.

The semianalytical approaches include the dimension-reduction technique (DRT) [9] and techniques based on the domain decomposition method [35–37]. The principles of the latter two techniques will be briefly discussed as follows.

3.3.4.1. Dimension Reduction Technique. The DRT attempts to solve problems within the finite domain. Most VLSI interconnects have stratified structures, and every layer is homogeneous along the direction perpendicular to the interfaces of the layers (denoted as the z direction; see Fig. 13). The DRT takes full advantage of this fact. It first partitions the whole structure according to these homogeneous layers. Then, for each layer the 3D Laplace equation can be reduced to a 2D Helmholtz equation, which is solved with the most efficient method (including the analytical formula) according to the arrangement of the conductors. Finally, the solutions for these cascading 2D problems are combined together to yield the final result.

For the finite-domain problem of the ith layer with Eq. (8), denote $W^{(i)}(x, y, V_c)$ as a linear function of x, y and the bias voltage setting on conductors (denoted by vector V_c), and let

$$u^{(i)} = v^{(i)} + W^{(i)}(x, y, V_c).$$

If there exists a function such as $W^{(i)}(x, y, V_c)$, that

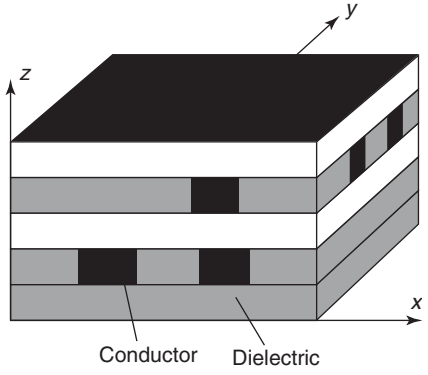

Figure 13. A 3D interconnect capacitor and the stratified layers.

function $v^{(i)}$ satisfies

$$\begin{cases} \nabla^2 v^{(i)}(x,y,z) = 0 \\ v^{(i)}(x,y,z) = 0, & (x,y) \in \Gamma_u^{(i)} \\ \partial v^{(i)}(x,y,z)/\partial \boldsymbol{n} = 0, & (x,y) \in \Gamma_q^{(i)} \end{cases}$$

then from the method of separation of variables, the general solution of $v^{(i)}$ is

$$v^{(i)}(x,y,z) = \sum_{m=1} T_m^{(i)}(x,y) L_m^{(i)}(z)$$

where $T_m^{(i)}$ is the mode function fulfilling the Helmholtz equation and $L_m^{(i)}$ can be solved analytically [9].

According to the conductor arrangement in the layer and the preceding analysis, the layer slices are classified as follows:

1. An Empty layer or a layer containing some simple conductors (such as that involving straight lines penetrating the structure) for which the linear function W and the analytical solution of the Helmholtz equation both exist.
2. The layer for which the linear function W exists, allowing the corresponding 3D problem to be transferred into the 2D Helmholtz equation.
3. A complex layer for which the W function does not exist. The 3D Laplace equation must be solved, but only the 2D finite-difference grid is utilized because of the geometry symmetry along the z direction.

The main drawback of the DRT is that the geometry it employs has some limitations; For instance, it is difficult to apply DRT to nonplanarized structures. So, for generalized and complicated interconnect structures using the DSM technology, the efficiency of DRT is not guaranteed.

3.3.4.2. Domain Decomposition Method. The domain decomposition method (DDM) is a newly developed numerical method. It can be subgrouped into the overlapping domain decomposition method (ODDM) and the nonoverlapping domain decomposition method (NDDM). The former is also called the *Schwarz alternating method* and the latter, the *Dirichlet–Neumann alternating method*. ODDM partitions the whole structures into some overlapped subdomains. Then, a global iteration is used for the solution. Its principles are discussed below [35].

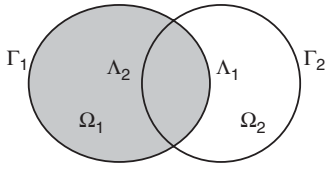

Figure 14. Two overlapping subregions.

Consider a 3D finite domain Laplace problem with the Dirichlet boundary condition

$$\begin{cases} \nabla^2 u = 0, (x,y,z) \in \Omega \\ u\big|_\Gamma = g(x,y,z) \end{cases}$$

Assume that the problem domain Ω involves two overlapping subdomains Ω_1 and Ω_2 (see Fig. 14), and denote Γ_j and Λ_j as the outer boundary and fictitious boundary of $\Omega_j (j = 1, 2)$, respectively. Then, the Schwarz alternating method is represented as

$$\begin{cases} \nabla^2 u_1^{i+1} = 0, & (x,y,z) \in \Omega_1 \\ u_1^{i+1} = u_2^i, & (x,y,z) \in \Lambda_1 \\ u_1^{i+1} = g(x,y,z), & (x,y,z) \in \Gamma_1 - \Lambda_1 \end{cases}$$

$$\begin{cases} \nabla^2 u_2^{i+1} = 0, & (x,y,z) \in \Omega_2 \\ u_2^{i+1} = u_1^{i+1}, & (x,y,z) \in \Lambda_2 \\ u_2^{i+1} = g(x,y,z), & (x,y,z) \in \Gamma_2 - \Lambda_2 \end{cases}$$

with $i = 0, 1, 2, \ldots$, where u^0 is the initial value for iteration. In each iterative step, the known values of u on Λ_1 are used to solve the field of subdomain Ω_1. Then, the field of subdomain Ω_2 is resolved with the u obtained on Λ_2. The discrepancy of u on Λ_1 between two adjacent iterative steps is used as the criterion of convergence. A relaxation factor ω can be introduced to these formulas to accelerate the convergence. It is also obvious that the convergence rate of the Schwarz alternating method is closely related to the size of the overlapping region. Usually the iteration error decreases exponentially with increase in the ratio of the overlapping domain over the subdomain [35].

It is straightforward to extend the preceding formulas of two subdomains to the generalized case with more subdomains. In each iterative step an analysis similar to that used in DRT can be employed to achieve high efficiency. In the actual application to capacitance extraction, the iteration sequence and selection of relaxation factor need to be considered. Figure 15 shows a cross-

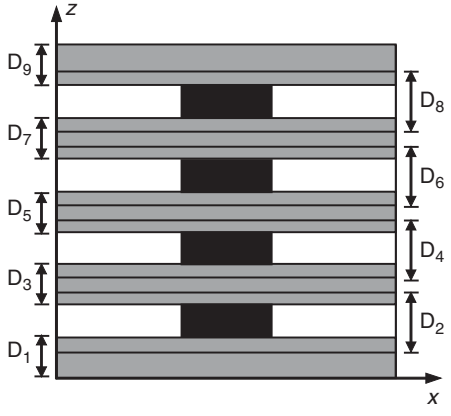

Figure 15. Four conductors embedded in nine dielectric layers.

sectional view of an interconnect capacitor with nine layers, and the domain partition scheme is illustrated.

In the NDDM technique, the decomposed subdomains do not overlap each other, while the iteration algorithm is similar to that in ODDM; the difference is that in the adjacent subdomains the problem is solved with the Dirichlet boundary condition and the Neumann boundary condition, respectively, in the NDDM. In NDDM, there are fewer unknowns in the subdomain, and sometimes only 2D discretization is needed for a simple subdomain with homogeneous structure. However, the convergence rate of NDDM is slower than that of ODDM [36].

Research on capacitance extraction based on the domain decomposition method is still underway. More recent progress can be found in Ref. 37.

3.3.5. Other Methods. The measured equation of invariance (MEI) method can be considered as a variation of FDM. To solve the infinite-domain model of capacitance extraction, the MEI method terminates the meshes very close to the object conductors and still preserves the sparsity of the finite-difference (FD) equations. The geometry-independent measured equation of invariance (GI-MEI) is proposed for the capacitance extraction of the general 2D and 3D interconnects by using the free-space Green function only [13]. The MEI method has now been developed to the on-surface level, where a surface mesh is used to minimize the number of unknowns [14]. The stochastic method is based on the random-walk theory and can effectively handle complex 3D structures. Its most recent progress can be found in Ref. 38.

4. PERSPECTIVE

In this article, we reviewed the state of the art in capacitance extraction techniques. These methods are discussed mainly for the accurate analysis of VLSI interconnects. However, they can also be easily to applied to computer-aided design of microwave ICs. With the development of IC technologies, the following issues related to capacitance extraction are important:

1. 3D capacitance extraction (i.e., 3D field solution) has the highest computational accuracy, and is suitable for complex interconnect structure under the DSM technologies. Many accelerating techniques have been developed to improve its speed. However, it is yet not feasible to use the 3D field solver directly in the full-chip extraction task. More effort should be devoted to improving the computational speed of the 3D field solver, or to develop special techniques for the full-chip task. The full-chip extraction method employing the 3D field solver would give both high computational speed and high accuracy.
2. Currently, few 3D capacitance extraction methods can be "tuned" for performance versus accuracy. The error estimation of the boundary-element method is also not established for practice. To make the 3D field solver suitable for various applications, its flexibility in tradeoff of accuracy versus computational performance must be improved. The adaptive algorithm and stable element partition scheme will be the focus of research in the future.
3. Mixed-signal integrated circuits have been demonstrated to provide high-performance system solutions for various applications such as wireless communications. Also, the silicon-based CMOS technology is increasingly widely used because of the fabrication cost advantage. To consider the significant impact of the lossy nature of the silicon substrate on the on-chip interconnects of the mixed-signal ICs, the frequency-dependent parameters of interconnects in high-speed circuits must be extracted accurately. Defining the complex permittivity of a material, the parasitic capacitance and conductance in a frequency-dependent model can be extracted using methods similar to that employed for traditional capacitance extraction. The most efficient algorithms for frequency-dependent capacitance extraction should be considered.

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