On-Chip Power Network Optimization with Decoupling Capacitors and Controlled-ESRs

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Abstract-In this paper, we propose an efficient approach to minimize the noise on power networks via the allocation of decoupling capacitors (decap) and controlled equivalent series resistors (ESR). The controlled-ESR is introduced to reduce the on-chip power voltage fluctuation, including both voltage drop and overshoot. We formulate an optimization problem of noise minimization with the constraint of decap budget. A revised sensitivity calculation method is derived to consider both voltage drop and overshoot. The sequential quadratic programming (SQP) algorithm is adopted to solve the optimization problem where the revised sensitivity is regarded as the gradient. Experimental results show that considering voltage drop without overshoot leads to underestimating noise by 4.8%. We also demonstrate that the controlled-ESR is able to reduce the noise by 25% with the same decap budget.

I Introduction

With aggressive technology scaling, power network has become one of the major concerns in VLSI design. The power supply voltage has been reduced to less than 1V, while the clock frequency is beyond multi-giga Hertz (GHz). The power network is experiencing unprecedented noise, which causes significant delay variation of devices, or even logic failure. Therefore, robust and reliable on-chip power supply network has increasing importance for high-speed circuit performance [1]. Optimizing the power network to confine the voltage fluctuation (including both droop and overshoot) so as to meet a target of noise tolerance (typically 5%~10% of nominal Vdd) becomes an essential step of on-chip circuit design.

Adding decoupling capacitors (decap) between the power network and the ground is an effective and widely adopted approach to reduce the power network impedance and therefore reduce the power network noise. Optimization with decap has two steps. The first one is to pre-place decaps before placing the standard cells. The second step is a post-placement refinement to the existing floorplan in an incremental manner. The focus of this paper is on the second step when the entire chip design is completed and current information is known. However, decap consumes die area and affects die yield adversely [2]. To control its negative impact, the total amount of decaps needs to be restricted while the decap locations are determined optimally to reduce the noise.

Most of existing research works for on-chip power noise reduction optimized the location and/or the amount of decaps. The optimization approach can be generally classified into two groups: the charge based algorithms and the sensitivity based algorithms. The charge based approaches estimate the total charge drawn from the power network during the worst-case switching scenario, and then determine the amount of decaps needed [3-5]. Recent works focused more on the sensitivity based approach. An adjoint network method is applied to calculate the sensitivity of the violation area for circuit node with respect to decap change [7, 8]. The sensitivity is used as the gradient in the nonlinear optimization solver. Because the number of simulations required for each iteration step is proportional to the number of nodes checked for violation, the computational complexity could be very high. To reduce the computational complexity, the merged adjoint network method was introduced and applied to calculate the sensitivity of the overall violation area with respective to decap [9, 10]. The idea is based on the superposition principle of linear circuits.

A concept of controlled equivalent series resistor (controlled-ESR) was recently proposed for on-chip [11] and off-chip power network design [12, 13]. It has been demonstrated that the controlled-ESR is effective to suppress the resonance, and reduce the simultaneous switching noise (SSN) as well [11, 12]. In [11], the decap with controlled-ESR was implemented in a CMOS process, and the controlled-ESR was adaptively changed to reduce the on-chip SSN.

In this work, we optimize the general on-chip power network with the usage of controlled-ESR. The noise of on-chip power network is minimized via the allocation of both decaps and controlled-ESRs. Different from previous works, we also consider the voltage overshoot when evaluating power network noise. Actually, excessive overshoot can cause system failure, and damages both the power supply and the loads coupled with it [18, 19]. We formulate the optimization problem with a constraint of decap budget, instead of minimizing the total amount of decap. Note that in contemporary power network designs it is impossible or unnecessary to completely remove the voltage violation. Muhtaroglu et al. [6] illustrated the trend that they devised an on-die droop detector instead of assuming a within the specification power supply. The optimization problem is solved with the sequential quadratic programming (SQP) algorithm. Experimental results show that the optimization algorithm is efficient, and the noise is reduced by 25% on average via the allocation of both decaps and controlled-ESRs. The main contributions are summarized as follows:

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(1) We propose to allocate decaps and controlled-ESRs simultaneously to suppress the resonance and reduce SSN of power network.
(2) We consider both voltage drop and overshoot for voltage violation. A revised sensitivity approach is presented to calculate the sensitivity the overall violation area with respective to both decap and controlled-ESR.
(3) An optimization formulation with the objective function of minimizing the voltage violation area and a constraint of decap budget is presented, and solved with an efficient SQP algorithm.

II Power Network Model With Controlled-ESR

The power network is usually modeled as a circuit including resistance, capacitance and packaging inductance, as shown in Fig. 1. The controlled-ESRs and decaps are connected between power grid nodes and the ground. Time-varying current sources are connected to some circuit nodes, characterizing the supply current for active circuit instances. These current sources draw current from the power network and cause voltage fluctuations [14]. The waveform of current source is described as a piecewise linear (PWL) function.

The controlled-ESR is able to effectively reduce the SSN especially when there is resonance phenomena caused by both the off-chip inductance and the on-chip capacitance [11]. However, if there are excessive controlled-ESRs, the impedance of power network will increase causing large SSN. A simplified model of power network with controlled-ESR is shown in Fig. 2. Fig. 3 shows the effect of controlled-ESR with different values on

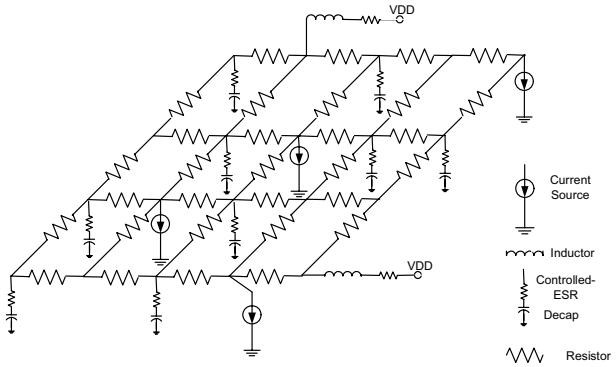

Figure 1. Power network model with controlled-ESR.

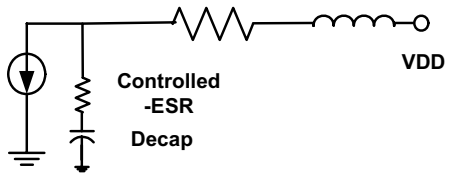

Figure 2. A simple case to show the effect of controlled-ESR.

reducing the noise. As the value of controlled-ESR increases from 10 mOhm to 1 Ohm, the noise is gradually reduced. But when there are excessive controlled-ESRs such as 10 Ohm, the noise (dash line) will become even larger. Therefore, we need to decide the adequate amount of controlled-ESRs.

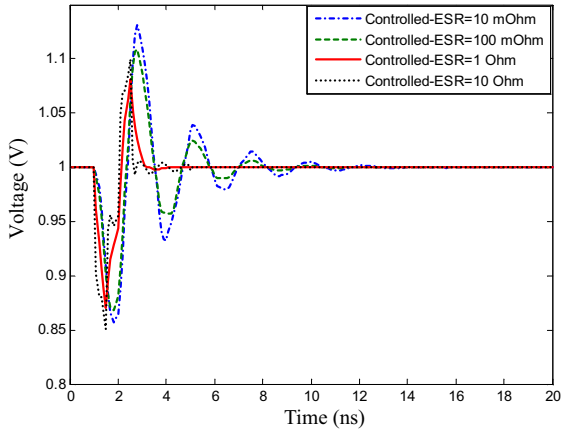

Figure 3. Effect of controlled-ESR on reducing the noise.

III Problem Formulation

We formulate the noise minimization problem as a nonlinear optimization problem. In this section, we first introduce the noise definition considering both voltage drop and overshoot. Then, the problem formulation including the objective function and constraints are presented.

A. Power Network Noise with Overshoot Consideration

Most existing works consider the power network noise as the violation area at circuit node. The violation area at node j is defined as:

$$g_j = \int_0^T \max(V_{\min} - v_j(t),\ 0)dt \quad , \tag{1}$$

where V_{min} is a pre-defined threshold voltage, and $v_j(t)$ is the voltage curve of node j. The violation area g_j equals to the shaded area below V_{min}. (see Fig. 4) This definition only considers the violation area below the nominal Vdd, as shown in Fig. 4, and neglects the voltage overshoot. The voltage overshoot is a transient rise of output voltage beyond Vdd. Excessive overshoot will lead to logic failure or the reliability issues. Therefore, the existing works underestimated power network noise due to the neglect of voltage overshoot.

In this paper, we consider both voltage drop and overshoot as the power network noise. The total violation area is defined as:

$$g_j = \int_0^T \max[\max(V_{\min} - v_j(t),\ 0),\ \max(v_j(t) - V_{\max},\ 0)]dt\,, \tag{2}$$

where $V_{\max}$ is a pre-defined threshold voltage above Vdd. With this definition, the violation area equals to the shaded area shown

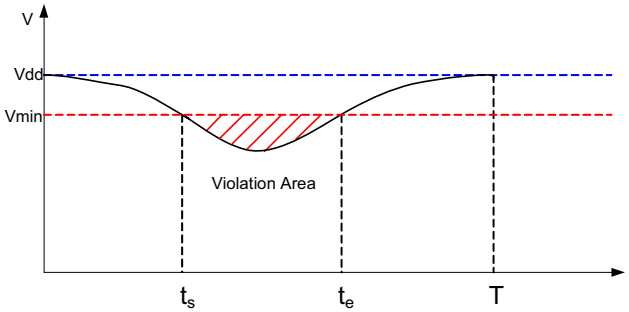

Figure 4. Voltage violation area with only voltage drop considered.

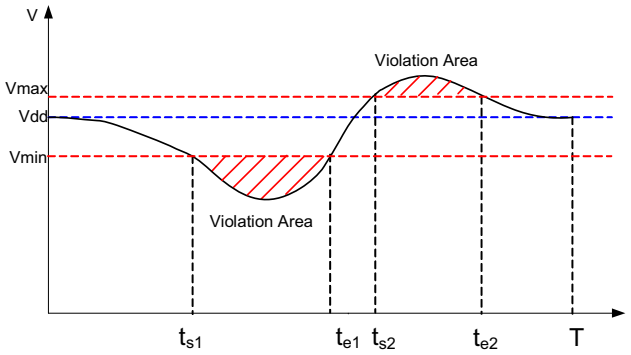

Figure 5. Voltage violation area with both voltage drop and overshoot considered.

in Fig. 5.

B. Formulation of Optimization Problem

For the power network optimization, the objective function is to minimize the total power network noise, which is the total violation area caused by both voltage drop and overshoot. The decision variables are the amount of decap and controlled-ESR at each candidate location: c_i and $CtrlESR_i$, $1 \le i \le M$. Here M denotes the number of candidate locations. We assume the power network stimulus is given. There are four constraints. The first one is that the voltages on nodes satisfy the circuit equation with given stimulus. With the transient voltage response, the violation area is then determined by equation (2). The second constraint is the total decap budget. The summation of all decap amounts should be not larger than a pre-defined budget Q. The third and forth constraint are the white space limitation for each candidate position. They mean that the amount of decap and controlled-ESR can not exceed the maximum allowed value. The formulation of the optimization problem is shown in Fig. 6.

Unlike minimizing the total decap with constraint of zero voltage violation in previous works, we minimize the total area of voltage violation with decap value as constraint. Considering the scale and complexity of the state-of-art power network design, it has become expensive and challenging to make the design totally free from voltage violation. Instead, recent industrial practices try to minimize the violation with given resource budget and to monitor the noise with sensors [6]. We do not set budget for the controlled-ESR since it is much cheaper than decap from silicon area perspective. The decap budget can be adjusted to evaluate the tradeoff between decap investment and noise elimination. Thus, the proposed formulation is reasonable and flexible.

Objective function:

$$\text{Min} \sum_{j=1}^{N} g_j$$

Constraints:

(1) Voltage response satisfies the circuit equation with given stimulus;

(2) Total decap budget: $\sum_{i=1}^{M} c_i \le Q$;

(3) Space constraint for each decap location: $0 \le c_i \le c_{\max i}$;

(4) Space constraint for each controlled-ESR location: $0 \le CtrlESR_i \le CtrlESR_{\max i}$.

Figure 6. Problem formulation of noise minimization of power network via allocation of decaps and controlled-ESRs.

IV Revised Sensitivity Computation

To solve the problem of power network noise minimization, the sensitivity value of the objective function to each decision variable is needed as the gradient in the procedure of nonlinear optimization. In this section, we firstly derive the voltage variation due to decap and controlled-ESR from the view of circuit state equation, and then review the merged adjoint network method to calculate the sensitivity of voltage violation area with respect to decap. Lastly, the revised sensitivity computation is presented, which considers the voltage overshoot and includes the controlled-ESR as the decision variable.

A. Voltage Variation Analysis with Circuit State Equation

In this section, we derive how the added controlled-ESR affects the voltage variation in a general power network. From Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL), we have the state equations:

$$\begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} \dot{v} \\ \dot{i} \end{bmatrix} = \begin{bmatrix} -G & -E \\ E^T & -R \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} + BU \ , \quad (3)$$

where C is the capacitance matrix, L is the inductance matrix. v is the voltage in each node and i is the current through every branch with inductance. G and R are conductance and resistance matrix, respectively. U is the input vector such as current source. We can get every node voltage and branch current by solving this equation.

We denote equation (3) to be

$$C\dot{x} = Ax + Bu \quad . \quad (4)$$

If we add some extra decap ΔC and controlled-ESR ΔA to the circuit, the solution vector x will be updated by Δx. And then, the state equation (4) becomes

$$(C + \Delta C)(\dot{x} + \Delta\dot{x}) = (A + \Delta A)(x + \Delta x) + Bu \quad . \quad (5)$$

By subtracting (4) from (5), we further get

$$(C + \Delta C)\Delta\dot{x} = (A + \Delta A)\Delta x + (\Delta A x - \Delta C\dot{x}) \quad . \quad (6)$$

The solution to the above differential equation (6) is

$$\Delta x = e^{\tilde{C}^{-1}\tilde{A}(t-t_0)}\Delta x_0 + \int_{t_0}^{t} e^{\tilde{C}^{-1}\tilde{A}(t-\tau)}\tilde{C}^{-1}\tilde{U}(\tau)d\tau \ , \quad (7)$$

where

$\tilde{C} = C + \Delta C$, $\tilde{A} = A + \Delta A$, $\tilde{U} = \Delta A x - \Delta C\dot{x}$, and

$$e^{\tilde{A}} = I + \tilde{A} + \frac{\tilde{A}^2}{2!} + \frac{\tilde{A}^3}{3!} + \ldots \ .$$

With (7), it is clear that the change of decap or controlled-ESR will have impact on the variation of voltage response. Because equation (7) is non-linear, we need to compute the sensitivity of voltage variation with respect to both decap and controlled-ESR for the optimization.

B. Sensitivity Computation with the Merged Adjoint Network Method

In existing works [1, 2, 6-10], the sensitivity computation only considers the violation area below Vdd as shown in Fig. 4. The sensitivity s_{ij} is defined to be the contribution of decap added at node i to remove violation at node j:

$$s_{ij} = \frac{\partial g_j}{\partial c_i} \quad , \quad (8)$$

where c_i is the decap value at node i, and g_j is the violation area defined in (1).

Because the computational complexity for standard sensitivity is very high, which requires N times of simulations (N is the number of violation nodes), the merged adjoint sensitivity is introduced to speed up the computation [9, 10]. The merged adjoint sensitivity is defined to be the contribution of decap added at node i to remove the violation for all nodes. An adjoint network is with the same topology as original network but with all of the voltage sources in the original network shorted and current sources open. The merged adjoint network has a current source $u(t-t_s)-u(t-t_e)$ applied at every node j if it is a node with noise defined in Fig. 4, where t_s is the starting time and t_e is the ending time of violation and $u(t)$ is the step function. With this method, the merged adjoint sensitivity is calculated with

$$s_i = \sum_{j=1}^{N} s_{ij} = \int_0^T (\tilde{v}_{i,all}(T-t)) \times \dot{v}_i(t)dt, \ (i=1,2,...,M) \quad , \tag{9}$$

where $\tilde{v}_{i,all}(T-t)$ is the voltage waveform at node i from the adjoint network with combined step current sources, $\dot{v}_i(t)$ is the derivative of the voltage waveform at node i in the original network. M is the number of candidate nodes to put decap. We need to set the initial condition of merged adjoint network to be zero and analyze backward in time.

C. *Revised Sensitivity Computation Considering Voltage Overshoot*

To consider voltage overshoot, the voltage violation area is defined as that shown in Fig. 5. We use the time points t_{sk}, t_{ek} to denote the starting and ending time of the kth violation, respectively. We need to calculate the sensitivity of the violation area defined in (2) to decap c_i and controlled-ESR $CtrlESR_i$, respectively.

It is convenient to extract all independent sources to form a multiport circuit. We denote the port currents and voltages by vectors I_p and V_p. Denote the non-source branch currents and voltages by vectors I_b and V_b. From Tellegen's theorem, we have

$$\int_0^T [-\hat{i}_p(\tau)\Delta v_p(t) + \hat{v}_p(\tau)\Delta i_p(t)]_{\tau=T-t}dt = \int_0^T [\hat{i}_b(\tau)\Delta v_b(t) + \hat{v}_b(\tau)\Delta i_b(t)]_{\tau=T-t}dt \quad , \tag{10}$$

where lowercase variables of i or v stand for the quantities of a specified port or branch. The symbols with hat (^) are for an adjoint network, those without hat are for the original network.

We set all voltage sources in the adjoint network to zero and apply a current source for each violation node:

$$I_s = \sum_{k=1}^{N_v} D_k[u(t-t_{sk}) - u(t-t_{ek})] \ , \tag{11}$$

where N_v is the number of violation stages on the voltage waveform (see Fig. 5), whose time intervals are (t_{s1}, t_{e1}), (t_{s2}, t_{e2}), …, $(t_{s,Nv}, t_{e,Nv})$. D_k is defined as:

$$D_k = \begin{cases} -1, & \text{if } v(t_{sk}) > \text{Vdd} \\ 1, & \text{if } v(t_{sk}) < \text{Vdd} \end{cases}, \ k=1, \ldots, N_v \, .$$

Then, the left hand side of equation (10) becomes

$$\Delta g = \int_0^T \left\{ -\sum_{k=1}^{N_v} D_k[u(t-t_{sk}) - u(t-t_{ek})]\Delta v_p(t) \right\}_{\tau=T-t} dt \cdot \tag{12}$$

This is exactly the derivative of violation area for voltage drop and overshoot.

The evaluation of the right hand side of equation (10) follows the same way as [17]. Then the sensitivity component for the decap is:

$$s_C = \frac{\Delta g}{\Delta C} = \int_0^T -[\hat{v}_c(\tau)\dot{v}_c(t)]_{\tau=T-t}dt \ , \tag{13}$$

and for the controlled-ESR is:

$$s_R = \frac{\Delta g}{\Delta R} = \int_0^T [\hat{i}_R(\tau) i_R(t)]_{\tau=T-t}dt \quad \cdot \tag{14}$$

The revised sensitivity computation method is described in Fig. 7. The input is the power network which needs to be optimized. The output is the violation area sensitivity with respect to each controlled-ESR and decap.

V SQP Based Optimization

We apply sequential quadratic programming (SQP) to solve the problem formulated in Fig. 6. The SQP is the state-of-the-art nonlinear programming method, which closely mimics Newton's method for constrained optimization just as is done for unconstrained optimization [15, 16]. For each iteration, the quasi-Newton updating method is used for the approximation of the Hessian matrix of the Lagrangian function. This approximation is then used to generate a quadratic programming (QP) subproblem. The solution for the subproblem is used to form a search direction for a line search procedure.

The SQP based optimization method is described in Fig. 8. The parameter $X^{(t)}$ is the solution of decap and controlled-ESR values in the t'th iteration. In our implementation, the noise sensitivities with respect to all the decap and controlled-ESR are computed

Algorithm for the revised sensitivity computation:

1. Simulate input circuit, and obtain a violation node set.
2. Obtain starting and ending time for each violation node shown in as Fig 5.
3. Obtain current $i_R(t)$ across controlled-ESR, and voltage derivation $\dot{v}_c(t)$ across decap in the original network.
4. Construct adjoint network, and apply the excitation described in Section *IV. C* to the adjoint network.
5. Simulate the adjoint network.
6. Obtain current $\hat{i}_R(\tau)$ across controlled-ESR, and voltage $\hat{v}_c(\tau)$ across decap in the adjoint network.
7. Evaluate the expression (13) and (14) to compute the sensitivity for each decap and controlled-ESR.

Figure 7. The algorithm description for revised sensitivity computation.

Algorithm for the SQP based optimization:

1. Select the intrinsic capacitance and controlled-ESR to be the initial solution $X^{(0)}$.
2. Simulate the power network circuit, and compute the sensitivity as gradient using the algorithm in Fig. 7.
3. Use the gradient to approximate the problem in Fig. 6 with a linearly constrained QP subproblem at $X^{(t)}$.
4. Solve for the step size $d^{(t)}$ to move.
5. If meet with termination condition, stop;
   Else, let $X^{(t+1)} = X^{(t)} + d^{(t)}$.
6. Increase t and return to step 2.

Figure 8. SQP based optimization method.

Table 1. Test cases description and the noise underestimation due to neglecting voltage overshoot

Circuit	# Node	Consider voltage drop only		Consider both voltage drop and overshoot		Noise underestimation due to neglecting overshoot
		Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	
CKT1	858	306.7	46	324.8	46	5.6%
CKT2	1794	7406.3	325	8127.8	347	8.9%
CKT3	2006	5111.3	309	5324.9	309	4.0%
CKT4	3634	9770.1	268	10049.6	268	2.8%
CKT5	8330	5608.1	2470	5829.1	2470	4.0%
CKT6	14852	31420.8	2243	32477.3	2243	3.4%

and are provided into the SQP algorithm as the first-order gradient, which is used to construct the QP sub-problem at each iteration. After solving this QP problem, the step size $d^{(t)}$ is determined to update the solution $X^{(t+1)}$. The termination criterion takes the value change of objective function, the step size, and the number of iteration into account. In the optimization, the total amount of controlled-ESRs is not restricted since it is relatively cheaper than decap. Therefore, higher priority should be made on allocating adequate amount of controlled-ESR than decap. Due to the sensitivity of violation area with respect to controlled-ESR is much smaller than decap, we need to scale the controlled-ESR sensitivity to get higher priority.

VI Experimental Results

The proposed SQP based optimization algorithm with revised sensitivity computation is implemented by Matlab and Perl. HSPICE is used to simulate the circuit. All experiments run on a 3GHz Pentium machine with 4GB memory.

Six cases of simplified industry on-chip power networks are tested. They are of mesh structure with R, C and packaging L. The number of nodes for each case varies from 858 to 14K, and is listed in the second column of Table 1. The nominal Vdd is 1.0V, and the allowable voltage fluctuation is 5%~10% of Vdd. In all experiments, we set the same noise tolerance ratio for voltage drop and overshoot.

A. Effect of Considering Voltage Overshoot

For each case, there are some intrinsic capacitors and controlled-ESRs. We firstly simulate these cases to reveal the effect of considering voltage overshoot on the voltage violation area. The value of noise, i.e. the voltage violation area and the number of violation nodes are listed in Table 1, with overshoot considered or not. As shown in the column 4 and 6 of Table 1, the number of violation nodes is almost the same for the both situations. However, the total noise is on average underestimated by 4.8% due to neglecting the voltage overshoot (compare column 3 and 5). Although the voltage drop noise still takes the major part of overall noise, the voltage overshoot should not be neglected in the noise model because it can lead to race condition and even logic failure.

B. Effect of Optimizing with Controlled-ESR

We then compare different optimization methods for the minimization of power network noise, with the same decap budget. In some industry design, decaps are evenly distributed at all candidate nodes. This method is straightforward, but definitely could not get the optimal solution. In the second method, the SQP based optimization described in Fig. 8 is employed but only the decaps are allocated. The third one is the proposed SQP based method allocating both decaps and controlled-ESRs. The comparison results are listed in Table 2. It is demonstrated that the number of violation nodes (column 3, 5, 7) is reduced, compared with the results in Table 1. And, the third method optimizing both decap and controlled-ESR yields the best solutions. For the noise, the third method also achieves the best solutions. The reduction on the minimized noise over the second method is listed in column 9 of Table 2, which shows that the improvement brought by considering the controlled-ESRs is 25% on average. With the third method, the average allocated controlled-ESR ranges from 0.038 Ohm to 0.083 Ohm for different cases.

Fig. 9 shows the voltage waveforms of one violation node in circuit CKT1 with the optimization methods applied or not. The dot-dash line is the waveform without optimization. The dash line is the waveform with even distribution of decap, which is better than the original waveform but still has higher noise than the SQP based optimization. The SQP method considering both decap and controlled-ESR is the best one which produces voltage response with less noise than the optimization considering decap only.

In Table 2, the CPU time is also listed for the proposed SQP based method allocating both decaps and controlled-ESRs. For the largest case with 14K nodes the total computational time is about 42 minutes. For each iteration, two HSPICE simulations run for the original and adjoint network, respectively, while the number of iteration is always less then twenty for the test cases. It is found out that the computational time is mainly spent by HSPICE simulation. With a faster simulation method for power network, the method would achieve faster computational speed.

C. Relationship between Decap Budget and Noise

To study the relationship between the minimal noise the optimization method can reach and the decap budget, we optimize the circuit CKT1 with different values of decap budget. The results are plotted in Fig. 10. The decap constraint ranges from 5nF to 50nF with a 5nF increment. The results show that larger

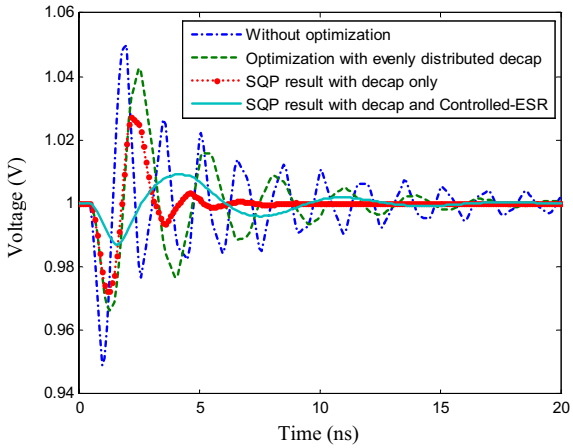

Figure 9. Voltage waveforms obtained with different optimization methods.

Table 2. Comparison among three methods for the minimization of power network noise

Circuit	Evenly allocate the decaps		Allocate decaps only with the SQP-based method		Allocate both decaps and controlled-ESRs with the SQP-based method			
	Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	Noise (V*ps)	# Violation node	CPU time (s)	Noise reduction compared to allocating decaps only
CKT1	229.5	20	113.4	23	82.1	16	26.2	27.6%
CKT2	6137.1	156	2538.0	104	2023.4	47	172.8	20.3%
CKT3	4597.9	141	2308.3	88	2077.2	78	116.7	10.0%
CKT4	8939.0	235	2212.5	96	1527.0	47	141.6	30.8%
CKT5	5352.3	1245	1694.3	617	1073.0	333	1195.2	36.7%
CKT6	26916.9	1191	6538.1	390	4853.6	204	2564.1	25.8%

decap budget leads to smaller noise. As more decaps are added, the benefit would increase slower (see Fig. 10). This relationship will help the designer to make the tradeoff between the noise reduction and the decap investment.

VII Conclusions

In this paper, we propose to allocate both decap and the controlled-ESR to optimize the on-chip power network. The objective function is to minimize the total voltage violation area including overshoot, and the optimization problem is solved with the SQP algorithm. The revised sensitivity computation considering voltage overshoot is derived to provide the gradient for SQP optimization. Experimental results demonstrate the necessity of considering the voltage overshoot, and adequately allocating the controlled-ESR is able to reduce the power network noise further by 25%, with the same decap budget. The optimization algorithm and the efficiency of controlled-ESR on chip area could be further investigated in the future.

VIII Acknowledgment

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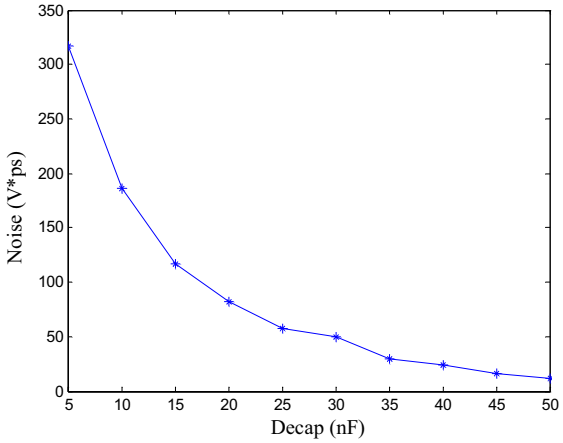

Figure 10. Relationship between decap budget and the noise.

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