Efficient Algorithms for Resistance and Capacitance Calculation Problems in the Design of Flat Panel Display

[**Invited Paper**]

Wenjian Yu[1] and Taotao Lu[2]

[1]TNList, Dept. Computer Science and Tech., Tsinghua University, Beijing 100084, China.

[2]Huada Empyrean Software Co., Ltd., Beijing 100102, China

Email: yu-wj@tsinghua.edu.cn, lutt@empyrean.com.cn

Abstract

Designing high-quality flat panel display (FPD) poses a couple of challenges to the electronic design community. To verify the equal signal delay on the wires to pixels and the validity of capacitive touch sensors, the resistance and capacitance of FPD structures should be accurately calculated. Two techniques, i.e. an analytical-BEM coupled resistance solver and a floating random walk based capacitance solver are presented. They efficiently resolve the resistance and capacitance calculation problems, and provide indispensable tools for the design of advanced FPD products.

1. Introduction

Flat panel display (FPD) has been a widespread and important human-computer interaction device in modern society. FPD evolves along two directions. One is very-large-area, high-brightness displays for home television and public information systems. The other is small-area, high-resolution, and low-power displays for mobile devices. The thin-film transistor (TFT) based active matrix technology is the basis of FPD. According to different lightening mechanism, the FPD employs the liquid crystal display (LCD) technique, or organic light emitting diodes (OLED) technique, etc. The substrate material is usually glass. Designing high- performance and low-cost FPDs is becoming an important topic in electronic design community [1-3].

A basic computer-aided design (CAD) design and verification flow of FPD includes steps of schematic design, circuit simulation, pixel design, layout design, layout verification and mask design (see Fig. 1). The panel layout verification includes the design rule check, electrical rule check, and the calculation of parasitic resistance, capacitance and voltage drop. To validate the signal timing and pursue high display quality, the resistance and capacitance of interconnect wires in FPD must be considered accurately. This problem is different from the parasitic extraction in VLSI circuit design. Firstly, the proximity of interconnects or between interconnects and the ground in FPD is much less than the proximity of VLSI interconnects [3]. Therefore, the parasitic capacitance in FPD is smaller and contributes less to the signal delay. Secondly, instead of pursuing small timing delay in circuit design, the most important

This work is supported by National Natural Science Foundation of China (No. 61422402).

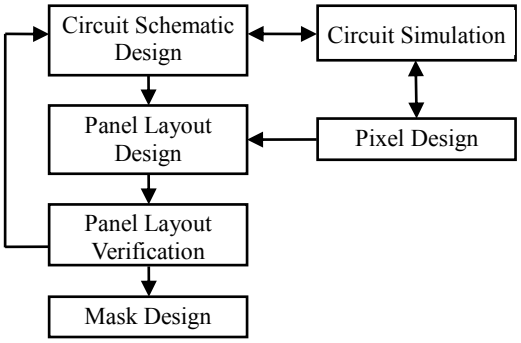

Fig. 1. A basic design and verification flow of FPD.

design and verification metric of FPD is keeping almost equal signal delay to all display pixels. This makes the wire resistance calculation important.

In recent years, touch panel (TP) technology has been combined with FPD to largely enhance the interactivity and user experience of various customer electronics. This kind of TP-FPD includes both the display components and touch sensor components. This makes its internal structure even more complicated. Most touchscreens utilize the capacitive touch sensor, due to its advantages in durability, reliability and capability [4]. To validate the functionality (like Multi-Touch, Force-Touch) and sensitivity of the touchscreen, accurately calculating the relevant capacitances becomes very important for the design of touchscreen FPD.

In this paper, we present two resistance and capacitance calculation techniques for high-quality FPD design. They are much more efficient than existing methods and well resolve the problems in FPD design.

2. A Hybrid Method for Calculating Wire Resistance

With the increase of resolution and the miniaturization trend, the narrow routing area in FPD contains more and more wires connecting the driver circuits and the TFT matrix. These interconnect wires have complicated geometry, largely different from that in IC design. Notice that the IC interconnects are mostly of simple geometry, e.g. aligned rectangles, whose resistances can be calculated with a simple square-counting approach. In FPD, the planar manufactory technology is usually employed. So, the resistance calculation is a 2-D problem. Below, a fast and accurate method is presented.

2.1 The analytical-BEM coupled approach

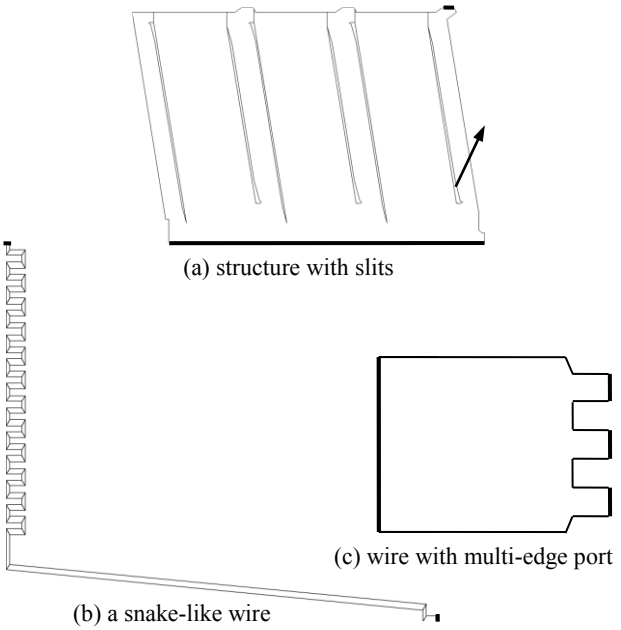

Fig. 2. Three typical FPD wire structures.

In Fig. 2, typical wire topologies of the FPD wire structure are shown. They have unaligned bevel edges, any-angle corners, and may include slits as well. The slits in Fig. 2(a) is used to increase resistance while not weakening the adhesion. The snake-like wire in Fig. 2(b) is also for increasing the resistance within a narrow routing area. The electrical resistance between the two bold edge segments needs to be calculated. Fig. 2(c) shows a special structure, where the right port consists of multiple disjoint edges.

For the irregular 2-D structure, its resistance can be solved with direct boundary element method (BEM). It only requires boundary discretization, producing smaller size but dense linear equation system [5]. To handle the complexity of FPD wire structures, an automatic boundary element partition approach is proposed. It employs nonuniform partition which involves fewer elements while preserving desirable accuracy [6]. However, for the long-wire structure like that in Fig. 2(b), BEM involves a lot of elements, and thus is inefficient. To settle this problem, we propose an analytical-BEM coupled approach. It follows the divide-and-conquer idea, which divides the wire into some portions with rectangle shape and the left portions. Then, the rectangle parts and the remain parts are solved with the analytical formula and BEM respectively. This is presented as Algorithm 1.

Algorithm 1: The analytical-BEM coupled approach

1: R := 0;
2: Calculate the tilt angle θ_i, (i=1, ..., n) of all outer-loop edges of the wire profile;
3: **For** i=1,...,n //n is the number of outer-loop vertices
4: **For** j=i+1,...,n
5: **If** $|\theta_j-\theta_i|<\theta_{tol}$, **then**
6: Calculate the valid rectangle;
7: **If** there is a rectangle with length/width ratio> η, **then**
8: Obtain a long-wire rectangle by cutting length of 3X width from the both ends of the valid rectangle;
9: Calculate resistance R_{rec} of the long-wire rectangle;
10: R:= R + R_{rec};
11: Cut off the long-wire rectangle, and adjust ports;
12: **Endif**
13: **Endif**
14: **Endfor**
15: **Endfor**
16: **For** each left portion of the wire,
17: Use BEM to calculate resistance R_{lef};
18: R := R +R_{lef};
19: **EndFor**

2.2 Numerical results

The presented approach is implemented into a C-based program *Res2d*. It involves LAPACK to solve linear equations derived from BEM. The experiments are carried out on a Linux server with Intel Xeon E5-2630 6-core CPU. The resistance of several FPD wires are calculated. We assume conductivity $\sigma = 1\ (\Omega\cdot\mu m)^{-1}$.

The results are listed in Table I. Our approach is compared with Raphael RC2 [7]. Raphael is the golden standard for the calculation of resistance and capacitance. It is based on finite difference method and employs an advanced nonuniform meshing scheme. Though it is widely used for IC industry, it is not efficient for the irregular wires in FPD. From Table I, we see that Res2d has high accuracy (error <1%), and its runtime is from 300X to 400X faster than Raphael.

Table I. The Resistance Results for Five Actual Cases in FPD

Case	Raphael RC2			Res2d			
	#grid	R (Ω·μm)	Time (s)	#element	R (Ω·μm)	Error (%)	Time (s)
1	703K	4.158	2513.4	3873	4.183	0.60	5.54
2	--	--	--	1547	261.2	--	1.48
3	100K	91.43	82.3	848	90.87	-0.61	0.25
4	57K	2.092	40.1	280	2.08	-0.57	0.01
5	--	--	--	3931	1770	--	5.92

3. Floating Random Walk Based Capacitance Solver

The capacitance calculation problem in TP-FPD design involves simulating the electrostatic field within the whole structure including touch sensor, surrounding FPD wires, and even the finger stylus. It calls for an accurate and efficient field-solver based solution. This problem is similar to the capacitance extraction problem in the design of VLSI circuits.

A lot of field-solver techniques have been proposed for accurate VLSI capacitance extraction, including domain discretization methods, BEM [8], and the floating random walk (FRW) method [9-13]. The first two involve volume or surface discretization and result in a system of linear equations, while the FRW method is based on the Monte Carlo method, and has the advantages of more scalability for very large structures, tunable accuracy, better parallelism, and much smaller memory usage. Furthermore, it is more reliable on accuracy than the BEM capacitance solvers. However,

the efficiency of FRW based techniques mainly depends on the assumption that the considered geometries are all of Manhattan shape, which is only true for VLSI circuits. Also notice that the aspect ratio (lateral dimension over thickness) of metal in FPD structures can be larger than 1000, which causes difficulty for the discretization based methods. This means there are distinct differences between the capacitance calculation problems in VLSI design and FPD design. Other differences lie in the dielectric configuration and the accuracy demand, as listed in Table II. The manufacturers of FPD are very diverse, which means a good capacitance solver for FPD verification should suit various configurations of dielectric material.

Table II. The Differences between VLSI Capacitance Extraction and Capacitance Calculation for TP-FPD Design.

	VLSI circuit capacitance extraction	**Touchscreen capacitance calculation**
Conductor geometry	Mostly Manhattan shape, with moderate aspect ratio	Generally non-Manhattan shape, with very large aspect ratio
Dielectric environment	On-chip dielectric insulators; relatively fixed dielectric profile	In-device dielectrics and out-device air; arbitrary dielectric configuration
Accuracy demand	Mainly self-capacitance for delay calculation	Need accurate coupling capacitances

Fig. 3 shows a typical dielectric profile and example conductor layouts (in top view) of the TP-FPD structure. In Fig. 3(a) we see that the top dielectric layer is air, i.e. the relative permittivity ε_5=1. And, the lateral dimension of a metal is usually much larger than its thickness. Fig. 3(b)~(c) show arbitrary-angle polygons and conductor with slits (holes). They include the geometries of a touch sensor and the wiring structures around it. The FRW method should be extended to handle these general non-Manhattan geometries, and this has been achieved with the techniques recently proposed in [12].

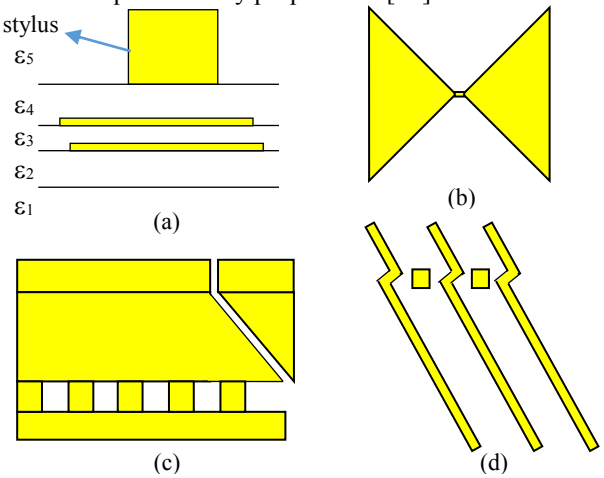

Fig. 3. (a): the cross-section view of a TP-FPD structure. (b)~(d): some examples of top-view layout of the structure.

3.1 A unified dielectric pre-characterization approach

A pre-characterization approach is called the dielectric homogenization method [9]. Its main idea is assuming that any cubic transition domain with multiple dielectric layers can be approximated by a cube with four equal-thickness dielectric layers, no matter how many dielectric layers it actually contains. In Fig. 4, we show a structure with five dielectric layers to illustrate different transition cubes and pre-characterization strategies. When employing the dielectric homogenization method, one can use the blue transition cube, whereas one has to choose the red one if the approach of [13] is used. So, the dielectric homogenization method brings better runtime efficiency to FRW, and it does not depend on the process technology. However, this four equal-thickness dielectric approximation may induce significant error while handling the structures with more dielectric layers [14]. And, it only suits the situation where the permittivity ratio of adjacent dielectrics is no larger than 2, which does not hold for the TP-FPD structure.

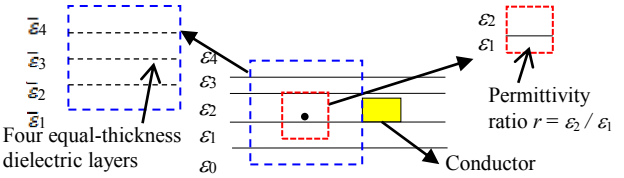

Fig. 4. An example for illustrating the transition cubes in the dielectric homogenization method and the proposed method.

To meet the requirements for simulating the TP-FPD structures, we propose to compute pre-characterization for arbitrary two-dielectric cube configurations and then employ two-dielectric transition cubes during random walks. As shown in Fig. 4, we consider different choices of permittivities (ε_1, ε_2) and the position of dielectric interface. Due to symmetry, we need only consider the situation where the two permittivities are (1, r), $0<r\leq 1$. Let s denote the smallest value of r, and N_{TDC} denote the number of sampling two-dielectric configurations. If we use equal-sized sampling of the r value, the number of samples is n= (1-s)/t+1, where t is the step size. For N-1 positions for dielectric interface, we finally get:

$$N_{TDC} = n(N-1) = (N-1)[(1-s)/t+1]. \quad (1)$$

If N = 31, s = 0.1, t= 0.015, this approach pre-calculates GFT/WVTs in size of about 177 MB, and it has already considered that the ratio of dielectric permittivity can increase to 10 in TP-FPD structures.

With this unified dielectric pre-characterization, we can handle any dielectric configuration. If the actual permittivity ratio r is between two sampled values: r_i and r_{i+1}, linear interpolation is employed to generate its corresponding GFT and WVT.

Three cases in TP-FPD design have been tested with the proposed technique [15]. They involve dielectrics with permittivity ranging from 1.0 to 7.0, and include layout patterns in Fig. 3. Some experimental results are listed in Table III. From the results we see that the homogenization approach produces large error for Case

3, and the proposed technique consumes much less memory and is very accurate.

Table III. The Computational Results of the FRW Algorithms with Different Dielectric Pre-Characterization Strategies.

Case	RWCap [13]		Proposed method			Homogenization [9]		
	Time	Mem.	Time	Mem.	Error	Time	Mem.	Error
1	2.3s	9.6MB	2.4s	12.4MB	<0.1%	2.8s	251MB	<0.1%
2	539s	5.7MB	530s	11.2MB	<0.1%	629s	250MB	<0.1%
3	222s	21MB	227s	34.7MB	0.01%	40.3s	273MB	-13%

3.2 Parallel simulation on a computer cluster

The computational time of the FRW algorithm is inversely propositional to the square root of number of walks. This means its runtime increases substantially with greater accuracy. For calculating capacitances during the touchscreen design, highly accurate coupling capacitances are required. But, there is not an efficient way to accelerate the calculation of coupling capacitances. So, a feasible way may be parallel computing. To this aim, we have developed the parallel FRW algorithm on a distributed computing environment.

To reduce the communication among computer nodes to the least, we propose to distribute the task through setting a suitable termination criterion of the FRW algorithm. As we know, the error of result

$$err \propto \frac{1}{\sqrt{N_{walk}}} \quad , \tag{2}$$

where N_{walk} is the number of FRW walks. If we have n_{proc} processes, then each process need run N_{walk}/n_{proc} walks. So, we can try to distribute the number of walks to each process at the beginning via setting new termination (accuracy) criterion to each process. With (2), we can derive that the new termination criterion for each process should be

$$err' = \sqrt{n_{proc}} \cdot err \quad . \tag{3}$$

The flowchart of the distributed FRW algorithm is shown in Fig. 5. Each process executes the random walk procedure independently tile the new termination criteria is reached. Then, the results of all processes are collected by the matster process to compute capacitance results.

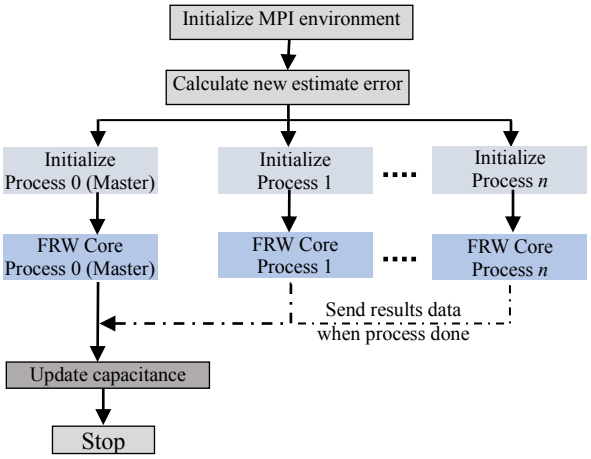

Fig. 5. The parallel FRW algorithm on a computer cluster.

We have implemented this algorithm in MPI on a homogenous computer cluster. Setting 0.1% 1-σ error as the accuracy criterion, the aforementioned three cases are simulated. The trends of parallel speedup vs. the number of processes are shown in Fig. 6. From it we see that with 120 processes, the speedup becomes 91X, 111X and 113X for the three cases, respectively. The proposed algorithm has much larger parallel efficiency than the distributed FRW algorithm proposed in [15].

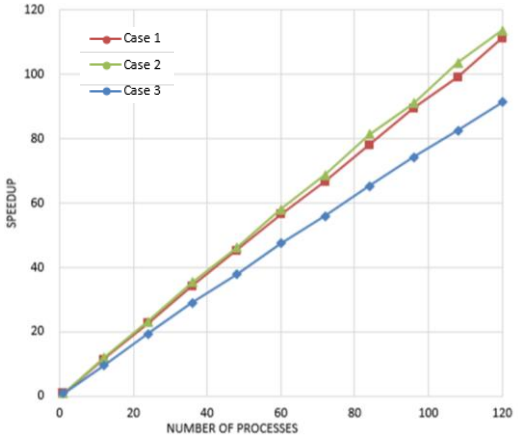

Fig. 6. The parallel speedup vs. the number of processes.

4. Conclusion

Efficient resistance/capacitance calculation techniques have been developed for the design of high-quality FPD. They have brought benefits to time-to-market and yield of FPD products, and will be further enhanced to tackle future challenges on structure complexity and accuracy.

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